

AS400-2A1 Series Server System

User Manual

Document Revision History

Version	Date	Description of Changes
0.9	2025/12/12	First Released
0.9a	2026/01/09	<ul style="list-style-type: none">• Updated System Feature Identification (Rear-Left View) table• Updated HPM Board Component table• Updated switch board power cable connection sequence• Added images of add-on card removal and installation procedures• Added Cable Routing and BIOS Setup sections• Add comments in the section “Appendix A: Hardware Information should be noted” and “Appendix B: Software Information should be noted”

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This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Safety Information

Safety Instructions

The equipment is intended for installation in a restricted access area, suitable for installation in Information Technology Rooms in accordance with Article 645 of the National Electrical Code and NFPA 75.

- Access can only be gained by service personnel about the reasons for the restrictions applied to the location and about any precautions that shall be taken.
- Access can only be gained with a tool or lock and key, or other means of security, and is controlled by the authority responsible for the location.
- This equipment should be installed and operated at a minimum distance of 8 inches/20 cm between the radiator and your body.
- Leave enough clearance (25 inches/63cm in the front and 30 inches/76 cm in the back of the rack) to allow the front door to be opened completely and to allow for sufficient airflow.
- Keep the area around the system clean and clutter-free.
- This product is not suitable for use with visual display workplace devices according to §2 of the German Ordinance for Work with Visual Display Units.

Warning

Only skilled personnel can remove the covers to access the inside of the system. Pay close attention to the following safety instructions before performing any of the operations to protect yourself from harm and the product from damage:

- Operation of the product should be carried out by suitably trained, qualified, and certified personnel only to avoid the risk of injury from electrical shock or energy hazards.
- Before starting the installation of the equipment, ensure that service personnel have attached an appropriate grounding lug to the grounding cable supplied.
- Place the system on a stable and flat surface.
- Disconnect the power cord from the wall outlet when installing or removing main system components, such as the motherboard.
- Use extreme caution when working with high-voltage components.
- When handling parts, use a grounded wrist strap designed to prevent static discharge.
- Keep all components and printed circuit boards (PCBs) in their antistatic bags when not in use.
- Handle a board by its edges only; do not touch its components, peripheral chips, memory modules or contacts.
- Only skilled people can remove the chassis covers to access the inside of the system.
- When removing the chassis lid required for servicing, turn off power and unplug any power cords/cables, and reinstall the chassis lid before restoring power.
- The power supply cord(s) must be plugged into socket-outlet(s) that is/are provided with a suitable earth ground.



Replaceable Batteries

Caution

Risk of explosion if battery is replaced by an incorrect type. Dispose of used batteries according to the instructions.

California, USA Only

The Lithium battery adopted on this motherboard contains Perchlorate, a toxic substance controlled in Perchlorate Best Management Practices (BMP) regulations passed by the California Legislature. When you discard the Lithium battery in California, USA, please follow the related regulations in advance.

Perchlorate Material-special handling may apply, see <https://dtsc.ca.gov/perchlorate/>

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Chapter 1 Introduction

This user manual is written for professional system integrators and server technicians. It provides information for the installation and use of the AS400-2A1 series server system. Installation and maintenance should be performed by experienced technicians only.

Chapter 2 Server System Overview

This chapter provides a general overview of the AS400-2A1 series server system. More in-depth information can be found in the following chapters.

There are two SKUs in the server system, configurations listed as below.

Table 1. System Configuration

SKU Name	GPU	NV NIC Card
AS400-2A1-RTX_PRO_6000	NVIDIA RTX PRO 6000	<ul style="list-style-type: none">4 pcs CX7 MCX755106AC-HEAT (dual port)1 pcs DPU B3220
AS400-2A1-H200_NVL	NVIDIA H200 NVL	



Figure 1. Server System Overview

2.1 Server System Specifications

The following table provides an overview of the features and available options supported by the AS400-2A1 series server system

Table 2. Server System Specifications

Feature	Details
Chassis Type	4U rack mount chassis
Chassis Dimensions	438 x 175 x 800 mm (W x H x D)
Processor Support	AMD EPYC 9005 Series (Turin)
Processor Socket Type	2 x sockets (SP5) Note: Previous generation AMD EPYC processor Genoa series are not supported.
Maximum Supported Processor Thermal Design Power (TDP)	Up to 400 W
GPU Support	8 x double-width GPU cards <ul style="list-style-type: none">• NVIDIA H200 NVL (TDP up to 600W, 4-way NV bridge support)• NVIDIA RTX PRO 6000 (TDP up to 600W)
Memory Slot	32 x DDR5 DIMM slots
Memory Support	<ul style="list-style-type: none">• Memory slots<ul style="list-style-type: none">○ 16 memory slots per processor, 8 memory channels per processor○ Two DIMM per channel• DDR5 RDIMM with two DIMM per Channel• All DDR5 DIMMs must support ECC• Memory capacity up to 2 TB per processor• Memory data transfer rates with DDR5 RDIMM (6400 MT/s rated):<ul style="list-style-type: none">○ Up to 5200 MT/s at one DIMM per channel○ Up to 4400 MT/s (1R) or 4000 MT/s (2R) at two DIMM per channel• DDR5 standard voltage of 1.1 V
System Fan Support	10pcs 8080 230W Fans (only support one rotor fan fail status)

Feature	Details
Power Supply Options	<ul style="list-style-type: none"> • The server system can support 4 pcs power supply modules configurations. • Depending on the power supply configuration, the system will support the following power operating modes: <ul style="list-style-type: none"> ○ 3+0 – single functional power supply ○ 3+1 – redundant power • Power supply options: <ul style="list-style-type: none"> ○ Total 4 pcs AC 3200-Watt Titanium CRPS with 4 pcs NVIDIA 600W GPU
Network Support	<ul style="list-style-type: none"> • AS400-2A1-RTX_PRO_6000 / AS400-2A1-H200_NVL SKU 4 pcs NVIDIA CX-7 dual ports and 1 pcs NVIDIA BlueField-3 3220 in PCIe Gen5 X16
Riser Card Support	<p>In the following description FH = Full Height, FL = Full Length, HL =Half Length, LP = Low Profile</p> <p>600W GPU supports the following options:</p> <p>AS400-2A1-RTX_PRO_6000 / AS400-2A1-H200_NVL SKU</p> <ul style="list-style-type: none"> • 8 pcs PCIe Gen 5 riser cables, which support <ul style="list-style-type: none"> ○ 8 pcs FH/FL double-width slot (x16 electrical, x16 mechanical) for NVIDIA H200 NVL / RTX PRO 6000 • 5pcs PCIe Gen 5 riser cables, which support <ul style="list-style-type: none"> ○ 3 pcs FH/FL single-width slot (x16 electrical, x16 mechanical) for NVIDIA CX-7 or B3140H ○ 1 pc HH/HL single-width slot (x16 electrical, x16 mechanical) for NVIDIA CX-7 or B3140H ○ 1 pcs FH/FL single-width slot (x16 electrical, x16 mechanical) for NVIDIA BF3 B3220
Onboard PCIe® NVMe® Support	<ul style="list-style-type: none"> • Supports up to 8 pcs PCIe NVMe • Two M.2 NVMe SSD connectors
Front Drive Bay Options	<ul style="list-style-type: none"> • 8 x Hot-swappable E1.S NVMe backplane • 2 x M.2 22110 / 2280 PCIe Gen3 x2 (NOT Support software RAID)
Buttons and LED Indicators	<ul style="list-style-type: none"> • Power button with LED • UID button with LED • System status LED • BMC reset button • E1.S hard drive status LED • Power supply unit status LED
Video Support	<ul style="list-style-type: none"> • Integrated 2D video controller • 64 MB of DDR4 video memory • One mini-DP connector on the front of the chassis, and can support VGA or HDMI through with active mini-DP to VGA or HDMI dongle cable

Feature	Details
USB Support	<p>One USB 3.0 connector on the front of the chassis</p> <p>Note: USB 3.0 port doesn't support USB3.0 Hub.</p>
Server Management	<ul style="list-style-type: none"> • Integrated Baseboard Management Controller (BMC) • One dedicated RJ45 1 Gigabit Ethernet (1 GbE) server management port • Intelligent Platform Management Interface (IPMI) 2.0 compliant • Redfish® compliant
Server Management Processor (SMP)	<ul style="list-style-type: none"> • Aspeed® AST2600 Advanced PCIe Graphics and Remote Management Processor • Embedded features enabled on this HPM board: <ul style="list-style-type: none"> ○ Baseboard Management Controller (BMC) ○ 2D video graphics adapter
Security Features	<p>Trusted platform module 2.0 (accessory option)</p>
BIOS	<ul style="list-style-type: none"> • AMI BIOS • Single SPI Flash
BMC	<ul style="list-style-type: none"> • AMI BMC • Single SPI Flash

2.2 System Feature Identification

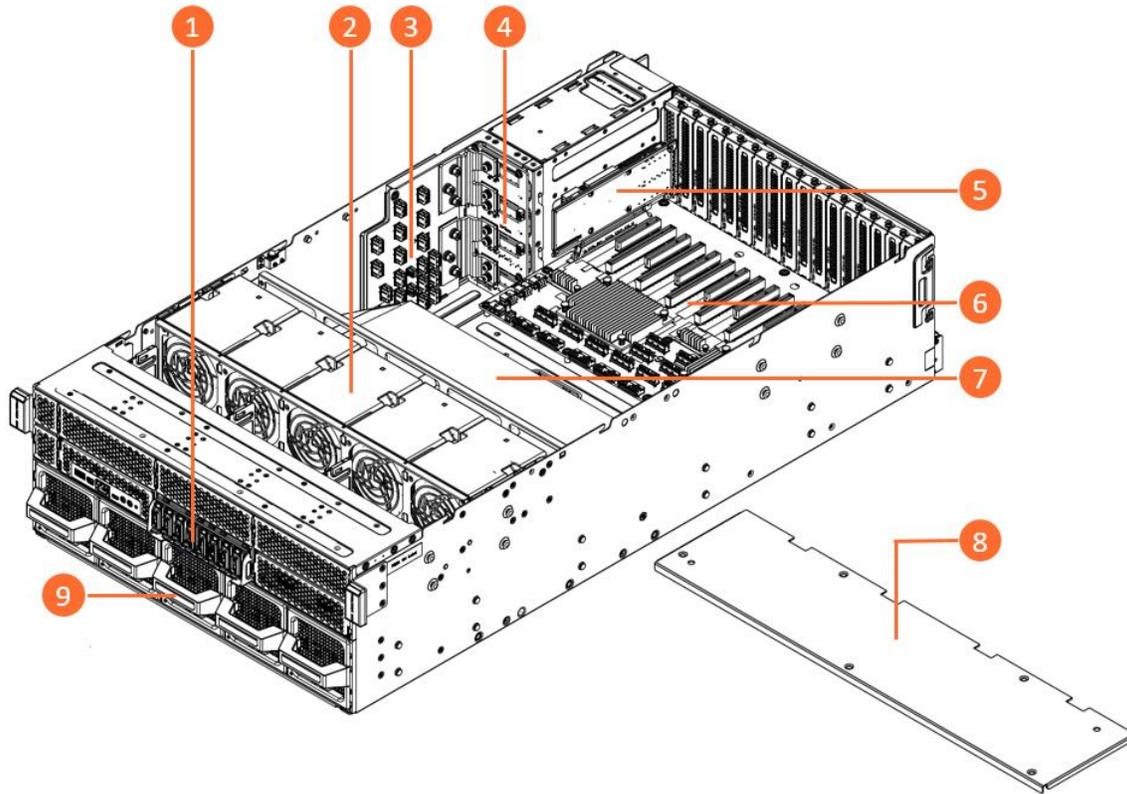


Figure 2. System Feature Identification (Front-Right View)

Table 3. System Feature Identification (Front-Right View)

No.	Description
1	E1.S drives
2	Top fans: V_FAN_0 to V_FAN_4 (from left to right at the system's front view)
3	Power distribution daughter board (PSD) #2
4	Power distribution daughter board (PSD) #1
5	FHFL PCIe card (e.g., NVIDIA CX-7 or B3140H NIC card)
6	PCIe Switch board (for up to 8 x double-width PCIe Gen5 x 16 GPU cards)
7	Air duct
8	GPU card cable support bracket
9	Front fans: R_FAN_0 to R_FAN_4 (from left to right at the system's front view)

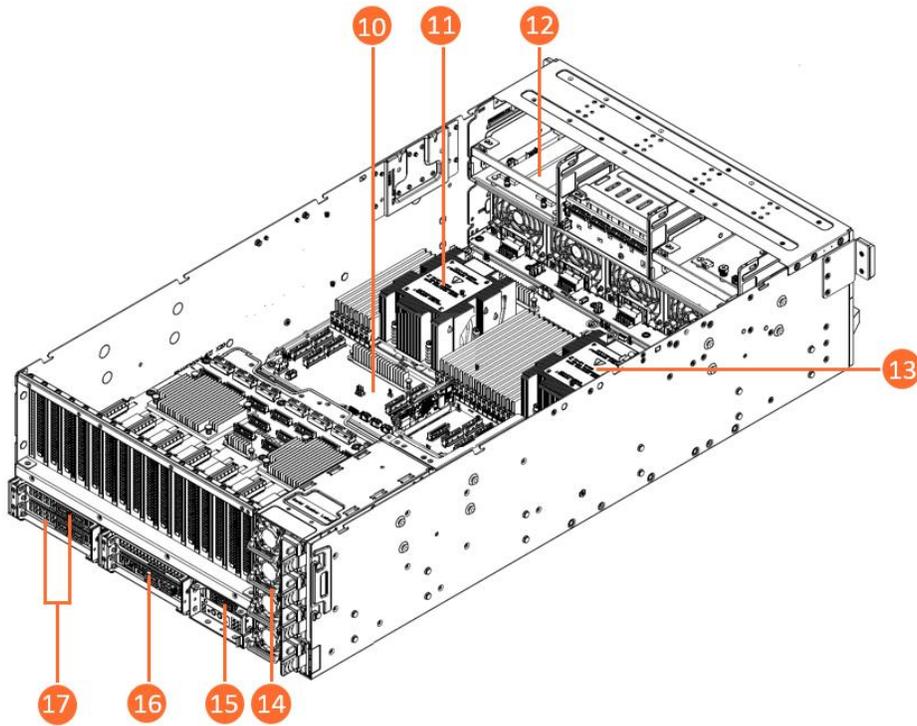


Figure 3. System Feature Identification (Rear-Left View)

Table 4. System Feature Identification (Rear-Left View)

No.	Description
10	Host Processor Module (HPM) board
11	CPU#1 heatsink
12	M.2 SSD slots
13	CPU#0 heatsink
14	Power supply units (PSU)
15	HHHL PCIe card (e.g., NVIDIA CX-7 or B3140H NIC card)
16	FHFL PCIe card (e.g., NVIDIA DPU BF3 B3220 card)
17	FHFL PCIe card (e.g., NVIDIA CX-7 or B3140H NIC card)

2.3 Front View

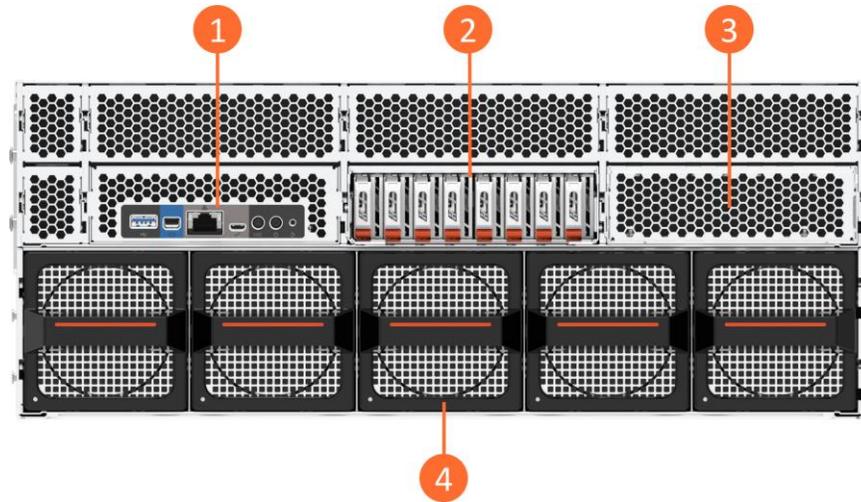


Figure 4. System Front View Features

Table 5. System Front View Features

No.	Description
1	<p>Front IO panel</p> <p>Note: Refer to section 2.4 Front Panel I/O and Buttons for more information.</p>
2	<p>Drive bay: 8 x E1.S NVMe (hot-swappable)</p> <p>Note: Refer to section 2.3.1 E1.S NVMe LED for LED definitions.</p>
3	2 x M.2 22110 / 2280 PCIe Gen3 x2 (NOT Support Software RAID)
4	Fan bay: 5 x 8080 fans

2.3.1 E1.S NVMe LED

Each E1.S NVMe drive features an amber LED that indicates its status.

Table 6. NVMe E1.S LED State Definition

LED State		Status
○	Off	OK
◐	4 Hz Blinking	Locate
●	Solid On	Fault
◑	1 Hz Blinking	Rebuild

2.4 Front Panel I/O and Buttons

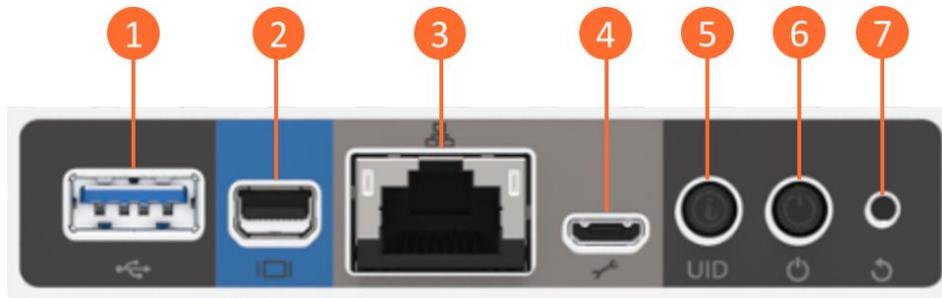


Figure 5. Front Panel I/O and Buttons

Table 7. Front Panel I/O and Buttons

No.	Description
1	USB 3.0 Type-A port
2	Mini DisplayPort
3	BMC indicated 1 Gigabit Ethernet RJ-45 port
4	Micro USB port for debugging (BMC debug console)
5	Unique Identifier (UID) button with LED
6	Power button with LED
7	Reset button

2.4.1 USB 3.0 type-A Port

The USB 3.0 Type-A port is integrated with USB 2.0 and does not support USB 3.0 hub.

Note:

USB 3.0 may generate Dmesg errors only in Ubuntu 22.04. These errors have not been observed in Redhat 9.2.

2.4.2 Mini Display Port

The server system features a Mini DisplayPort (DP) for video out and a VGA-compliant controller with 2D hardware acceleration and full bus primary support. The video controller supports the resolutions with mini-DP to DP/HDMI/D-sub dongle cable (purchased separately) in the following table.

Table 8. Mini DP Output Resolution

2D Mode Resolution	2D Video Mode Support (Color Bit)	
	16 bpp	32 bpp
640 x 480	60 Hz	60 Hz
800 x 600	60 Hz	60 Hz
1024 x 768	60 Hz	60 Hz
1280 x 800	60 Hz	60 Hz
1280 x 1024	60 Hz	60 Hz
1440 x 900	60 Hz	60 Hz
1680 x 1050	60 Hz	60 Hz
1920 x 1080	60 Hz	60 Hz

Note:

Please use an “active” Mini-DP to VGA or HDMI adaptor for video out to an external monitor.

2.4.3 BMC indicated 1 Gigabit Ethernet RJ-45 Port

The server system features a BMC dedicated 1 Gigabit Ethernet (GbE) RJ-45 port specifically designed for remote access to system management.

Refer to the table below for the LED behavior of the 1 GbE remote management port:

Table 9. Ethernet LED State Definition

Ethernet Status		Description			
		Left LED (Speed)		Right LED (Link/Activity)	
No Link	Off		Off		Off
Linked at 100 Megabit Ethernet (100 MbE)	Link		Solid amber		Solid green
	Active		Solid amber		Blinking green
Linked at 1 Gigabit Ethernet (1 GbE)	Link		Solid green		Solid green
	Active		Solid green		Blinking green

Note:

The system's management port does not support 10 Megabit Ethernet (MbE).

2.4.4 Micro USB Port

The Micro USB port is dedicated as a BMC UART debugging console only. There is a chance that some cables might not work due to power voltage. Please try to change to another cable and AC reboot to try again.

2.4.5 Front UID Button

The Unique Identifier (UID) button features a blue LED to identify the system in case of maintenance when installed in a rack of similar server systems. You can utilize the UID LED in one of the following methods:

- Press the button, causing the LED to illuminate to a solid-on state until the button is pushed again.
- Send an IPMI Chassis Identify command, causing the LEDs to blink for 15 seconds.

Table 10. Front UID LED State Definition

LED State		Description
	Solid blue	Activated
	Off	Deactivated

2.4.6 Front Power Button

Pressing this button sends a signal to the integrated BMC that either powers on or powers off the system.

Table 11. Front Power LED State Definition

LED State		Description
	Solid blue	System power on
	Off	System power off

Note: The system is configured to automatically power on when first connected to AC power. The power button will remain inactive until the BMC heartbeat LED indicates that the Baseboard Management Controller (BMC) is fully operational.

2.4.7 Reset Button

When pressed, this button reboots and re-initializes the system. Unlike the power button, the reset button does not disconnect the power to the system. It just starts the system's Power-On Self-Test (POST) sequence over again.

2.5 Rear View

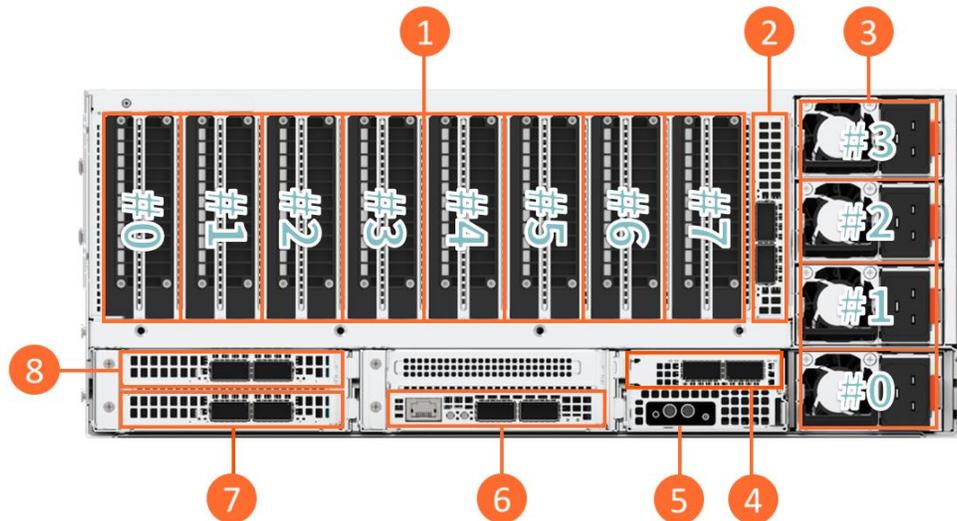


Figure 6. System Rear View Features

Table 12. System Rear View Features

No.	Description
1	8 x FHFL PCIe 5.0 slot for dual-slot GPUs, TDP up to 600W
2	1 x FHFL PCIe 5.0 x 16 slot (Add-on_4)
3	4 x Common redundant power supply (CRPS) Note: Refer to section 2.6 Power Supply Status LED for LED definition.
4	1 x PCIe 5.0 x 16 HHHL slot (Add-on_3)
5	Rear IO panel Note: Refer to section 2.7 Rear Panel Buttons and LED for LED definition.
6	1 x FHFL PCIe 5.0 x 16 slot (Add-on_2)
7	1 x FHFL PCIe 5.0 x 16 slot (Add-on_0)
8	1 x FHFL PCIe 5.0 x 16 slot (Add-on_1)

2.6 Power Supply Status LED

A single bi-color LED indicates power supply status. The operational states of this bi-color LED are defined in the following table.

Table 13. Power Status LED State Definition

LED State		Power Supply Condition
	Solid green	Output ON and OK.
	Off	No source of power to all power supplies.
	2 Hz blinking green	Power supply firmware updating.
	Solid amber	<ul style="list-style-type: none"> Source power cord unplugged, or source power lost; with a second power supply in parallel still with AC input power. Power supply critical events causing a shutdown; failure, over current protection, over voltage protection, or fan fail.
	1 Hz blinking amber	Power supply warning events where the power supply continues to operate; high temp, high power, high current, or slow fan.

2.7 Rear Panel Buttons and LED

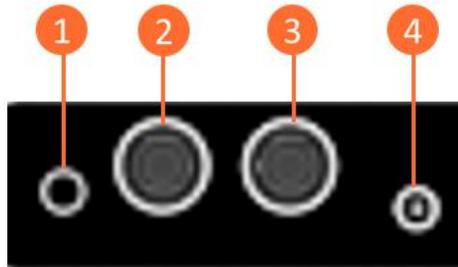


Figure 7. System Rear Panel Features

Table 14. Rear Panel Buttons and LED

No.	Description
1	Reset button
2	Power button with LED
3	UID button with LED
4	Status LED

2.7.1 Reset Button

When pressed, this button reboots and re-initializes the system. Unlike the power button, the reset button does not disconnect the power to the system. It just starts the system's Power-On Self-Test (POST) sequence over again.

2.7.2 Rear Power Button

Pressing this button sends a signal to the integrated BMC that either powers on or powers off the system.

Note:

The system is configured to automatically power on when first connected to AC power. The power button will remain inactive until the BMC heartbeat LED indicates that the Baseboard Management Controller (BMC) is fully operational.

Table 15. Rear Power LED State Definition

LED State		Description
	Solid green	System power on
	Off	System power off

2.7.3 Rear UID Button

The Unique Identifier (UID) button features a blue LED to identify the system for maintenance when installed in a rack of similar server systems. You can utilize the UID LED in one of the following methods:

- Press the button, causing the LED to illuminate to a solid-on state until the button is pushed again.
- Send an IPMI Chassis Identify command, causing the LEDs to blink for 15 seconds.

Table 16. Rear UID LED State Definition

LED State		Description
	Solid blue	Activated
	Off	Deactivated

2.7.4 Status LED

The system status LED is an amber indicator that shows the current health of the server system. The system status LED states are driven by the HPM board platform management subsystem. When the server is powered down (transitions to the DC-Off state or S5), the BMC is still on standby power and retains the sensor and front panel I/O LED state established before the power-down event. The following table provides a description of each supported LED state.

Table 17. System Status LED State Definition

Status LED		System Status	Description
	Solid on	Critical	<ul style="list-style-type: none"> • Critical threshold crossed – voltage, temperature and fan sensors • CPU CATERR • CPU configuration errors and thermal trip • None of the CPUs is present • Memory thermal trip • Uncorrectable memory ECC errors and configuration errors • Bus uncorrectable errors • PSU failure, input loss, or configuration errors
	Blinking	Warning	<ul style="list-style-type: none"> • Non-Critical threshold crossed – voltage, temperature, or fan sensors • Memory correctable ECC errors • Bus correctable errors • PSU predictive failure • Processor hot or Memory hot
	Off	Normal	<ul style="list-style-type: none"> • System power is not present • System status is Normal when system power is present

2.8.2 HPM Board Placement

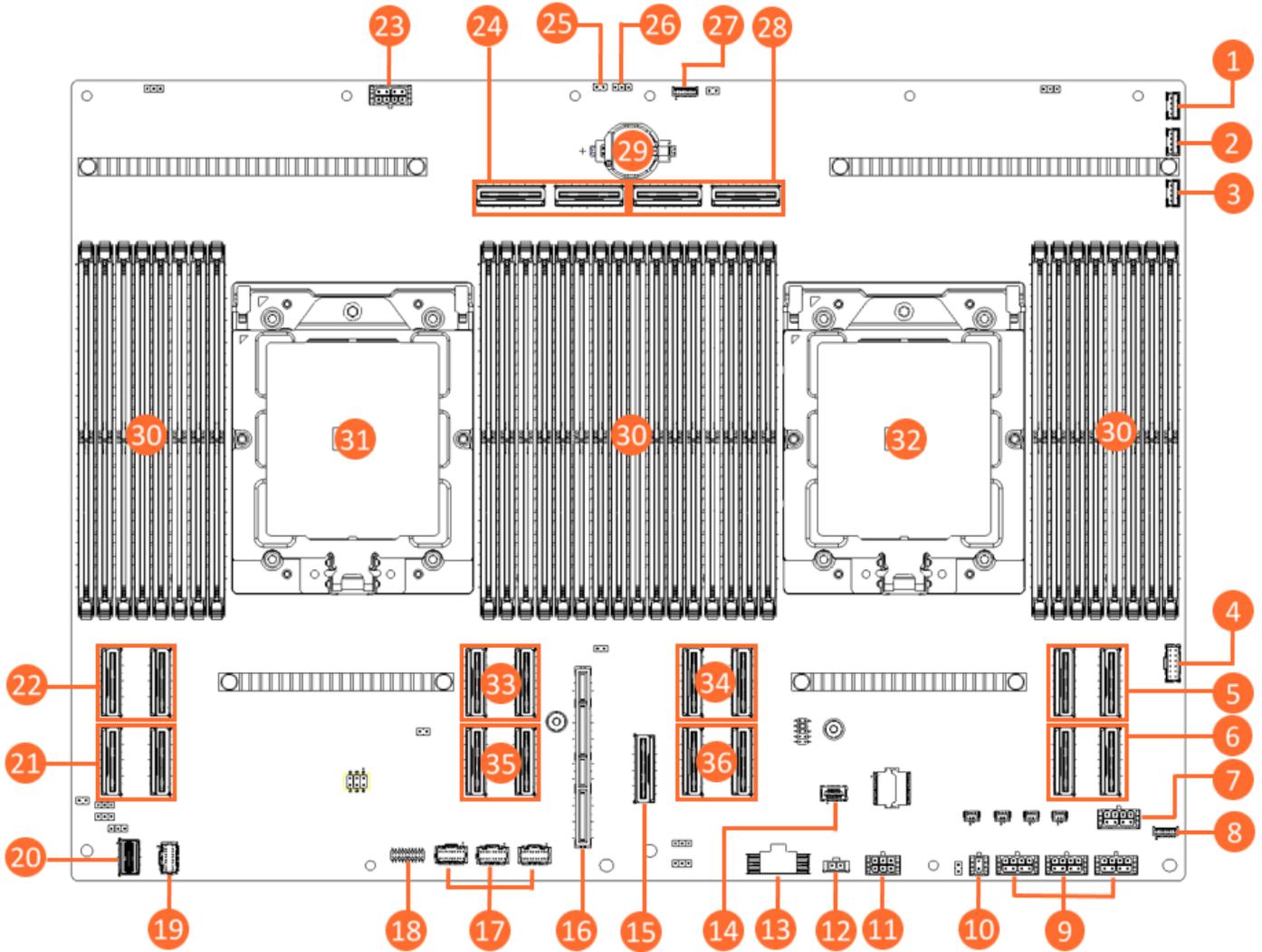


Figure 9. HPM Board Components

Table 18. HPM Board Components

Item	Header Reference	Description
1	BP_I2C_1	E1.S backplane sideband connector
2	BP_I2C_2	I2C for backplane connectors
3	BP_I2C_3	M.2 daughter board connector
4	J_IOBD	Rear IO daughter board sideband connector
5	MCIO0P0A, MCIO0P0B	CPU0 P1 (reserved)
6	MCIO0P1A, MCIO0P1B	Uses MCIO cable to PCIe switch board connectors (PCIe Gen 5 diff pairs)

Item	Header Reference	Description
7	J_NICPWR	Main power input for NIC
8	J_VTFAN1	Top fan daughter board connector
9	J_MBPWR1, J_MBPWR2, J_MBPWR3	Main power input for HPM board
10	J_MBSTBY	Standby power input for HPM board
11	J_BF3PWR	Add-on_2 card (BF3 card) power connector
12	J_IOPWR1	Front IO daughter board power connector
13	J_FARIO1	Front IO daughter board signal connector
14	CON1	TPM connector
15	MCIO0P4A	M.2 daughter board signal connector
16	NV_SCM1	NVIDIA DC-SCi
17	J_PDB_A1, J_PDB_B1, J_PDB_C1	Power distribution board side band connectors
18	J_HDT1	AMD hardware debut tool (HDT) connector
19	J_NCSI1	NC-SI for add-on_2 card (NVIDIA BF3 B3220)
20	J_NVHMC	NVIDIA software hardware management console (HMC) (Reserved)
21	MCIO1P3A, MCIO1P3B	CPU1 P3 (reserved)
22	MCIO1P2A, MCIO1P2B	Uses MCIO cables to PCIe switch board connectors (PCIe Gen 5 diff pairs)
23	J_BPM2PW	Main power input for backplane (E1.S/M.2)
24	MCIO1G1A,MCIO1G1B	MCIO from CPU 1
25	H_INTRUN	Intruder Note: Refer to Chapter 2.8.3 the System Configuration and Recovery Jumpers section for intrusion settings.

Item	Header Reference	Description
26	H_CLRRTC	Clear CMOS Note: Refer to Chapter 2.8.3 the System Configuration and Recovery Jumpers section for clear CMOS settings.
27	J_RAFAN1	Front fan sideband
28	MCIO0G3A, MCIO0G3B	MCIO from CPU 0
29	J_BATT1	CMOS battery
30	N/A	DIMM memory slots Note: Refer to section 2.9 Recommended System Memory Population for more information.
31	CPU1	CPU 1
32	CPU0	CPU 0
33	MCIO1P0A, MCIO1P0B	Uses MCIO cables to PCIe switch board connectors (PCIe Gen 5 diff pairs)
34	MCIO0P2A, MCIO0P2B	Uses MCIO cables to PCIe switch board connectors (PCIe Gen 5 diff pairs)
35	MCIO1P1A, MCIO1P1B	CPU1 P1 (reserved)
36	MCIO0P3A, MCIO0P3B	Uses riser cables to DPU (PCIe Gen 5 diff pairs)

Note:

Refer to **Appendix C** for connector pin definitions.

2.8.3 System Configuration and Recovery Jumpers

The HPM board is equipped with various jumper blocks that allow the configuration, protection, or recovery of specific features.

Table 19. System Configuration and Recovery Jumpers

Header Reference	Function	Jumper Placement
H_CLRRTC	CMOS Clear Header	<ul style="list-style-type: none">• 1-2: Normal (default)• 2-3: Clear CMOS
H_INTRUN	Intrusion Header	<ul style="list-style-type: none">• 1-2: Short <Chassis Closed>• 1-2: Open <Chassis Open >

Note:

Refer to the Chapter 2.8.2 **HPM Board Placement** section for the locations of jumpers.

2.9 Recommended System Memory Population

The server board features 32 DIMM slots, supporting the memory features below:

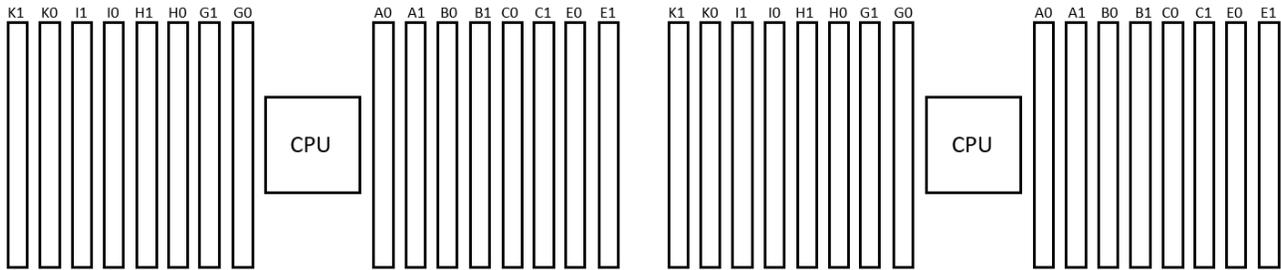
- DDR5 RDIMM (6400MT/s rated): 5200 MT/s when populated in DIMM 1; 4400 MT/s (1R) / 4000 MT/s (2R) when populated in DIMM 1 and DIMM0
- Support for 1-,2-, 4-, 6-, 8- and 16 memory interleaving
- RDIMM

The memory slots are designed with one memory channel for 2 DIMM slots (2 DIMM per channel). It is recommended to populate all DIMM slots with memory modules to maximize memory capacity and performance.

It's not allowed to use non-match capacity/speed across channels or to mix RDIMMs with non-ECC UDIMMs, to avoid boot failure / channel disabling or low performance.

Proper installation of DDR5 Registered DIMMs (RDIMMs) is critical for server stability and performance. Incorrect population or sequencing may cause boot failures, memory errors, or degraded functionality. For optimal memory performance, follow the instructions listed in the tables below when populating memory modules.

2.9.1 System Memory Population



DIMM	K1	K0	M1	M0	H1	H0	G1	G0	CPU	A0	A1	B0	B1	C0	C1	E0	E1	
1 DIMM												V						
2 DIMM							V					V						
4 DIMM			V				V					V			V			
6 DIMM			V		V		V					V		V	V			
8 DIMM	V		V		V		V					V		V	V	V		V
16 DIMM	V	V	V	V	V	V	V	V			V	V	V	V	V	V	V	V

Figure 10. Memory DIMM Population Table

Note:

Be sure to use the memory modules of the same type and speed on the motherboard. Mixing memory modules of different types and speeds is not allowed.

Populating memory slots with a pair of DIMM modules of the same type and size will result in interleaved memory, which will improve memory performance.

2.10 System Level Environmental Limits

Table 20. System Environmental Limits Summary

Feature		Details
Temperature	Operating	ASHRAE Class A2 – Continuous Operation. 10 – 35 °C (50 – 95 °F) with the maximum rate of change not to exceed 20 °C per hour in AS400-2A1-H200_NVL SKU. ASHRAE Class A2 – Continuous Operation. 10 – 30 °C (50 – 86 °F) with the maximum rate of change not to exceed 20 °C per hour in AS400-2A1-RTX_PRO_6000 and AS400-2A1-CX-8 SKU.
	Non-operating	-40 through 68 °C (-40 through 154.4 °F)
Altitude	Operating	TBC
	Non-operating	up to 39,370 feet (12,000 m)
Humidity	Operating	10% to 85%, non-condensing.
	Non-operating	Up to 93%, non-condensing.
Shock	Operating	For consecutively executed 3 shock pulses in the positive and negative x, y, and z axis of 3G for up to 11 ms.
	Unpackaged	Trapezoidal, 20G, 11ms. Velocity change is based on system weight (Bottom Side Only).
	Packaged	The package drop tests (Edge Drop, Corner Drop, and Free Fall Drop with pallet) were performed based on the drop test conditions specified in ISTA 3B.
Vibration	Operating	0.21 Grms at 5 Hz to 500 Hz for 20 minutes (all x, y, and z axes)
	Unpackaged	2.09 Grms at 5 Hz to 500 Hz for 30 minutes (Bottom Side Only)
	Packaged	1.48 Grms at 5 Hz to 200 Hz for 30 minutes (Bottom Side Only)
AC-DC (CRPS)	Voltage	Only support high line 180–264 Vac (rated 200–240 Vac) AC power in. NO support low line 90–140 Vac (rated 100–127 Vac) AC power in.
	Frequency	47–63 Hz (rated 50/60 Hz)
	Source interrupt	No loss of data for power line drop-out of 7 msec
	Surge and operating	Electromagnetic Compatibility (EMC) - Testing and measurement techniques - Surge test: +/-2KV common mode and +/-1KV differential mode for AC ports and meet IEC/EN61000-4-5 requirement

Feature		Details
	Line to earth only	AC Leads 2.0 KV I/O Leads 1.0 KV DC Leads 0.5 kV
ESD	Air discharged	+/-8kv @ Criterion B
	Contact discharge	+/-4kv @ Criterion B
Acoustics Sound Power Measured	Power	<300 W ≥300 W ≥ 600 W ≥ 1000 W
	Servers/rack mount Sound power level	7.0 BA 7.0 BA 7.0 BA 7.0 BA

2.11 System Packaging

The original system packaging is designed to provide protection for a fully configured system and tested to meet International Safe Transit Association (ISTA) Test Procedures 2A (2008) and 3B (2017). The packaging is designed to be reused after the integration of system components has been completed and the system is to be shipped to its destination.

The boxes and packaging components are designed to function together as a protective packaging system. When reused, the original packaging material must be free of any damage sustained from previous use.

Note:

The design of the inner packaging components does not prevent improper placement within the packaging assembly. Only one correct packaging assembly allows the package to meet the International Safe Transit Association (ISTA) Test Procedures 2A (2008) and 3B (2017) limits.

Failure to follow the specified packaging assembly instructions may result in damage to the system during shipment.

The outer shipping box dimensions are:

- Length: 1200 mm
- Width: 800 mm
- Height: 409 mm

2.11.1 Package Contents

- 1 x Server system
- 4 x Chassis handle
- 4 x AC power cord
- 1 x Rail kit box
- 2 x Heatsink for CPU
- 2 x Removal tool

Note:

The L10 package contents may vary based on your actual purchase order.

Please contact your distributor if there is anything missing or damaged.

Chapter 3 System Power - CRPS (Common Redundant Power Supply)

The server system supports 4 pcs AC 3200W (Titanium) for 8 pcs 600W GPU (e.g., H200 NVL / RTX PRO 6000).

Note:

System power only supports high line 180–264 Vac (rated 200–240 Vac) AC power in. **NO support for low line 90–140 Vac (rated 100–127 Vac) AC power in.**

3.1 Power Supply Configurations

Embedded platform management automatically determines and configures the power supply configuration based on the number of functional power supplies detected, and the total power draw of the system.

The system supports the following power configurations:

- 3+0 – Three power supply units (PSUs) are installed and operational. This configuration provides no power redundancy. The system will operate normally only if the total power requirement remains within the maximum combined capacity of the three functional PSUs.
- 3+1 – Four power supply units (PSUs) are installed and operational. This configuration provides N+1 power redundancy (single failure protection). The system will maintain full operation even if one PSU fails, as long as the total power requirement remains within the maximum combined capacity of any three functional PSUs. Hot-swap replacement of failed units is supported.

Note:

In a redundant power supply 3+1 configuration, 4 pcs power supplies must be identical. A system configured with different power supply options is not supported. An unsupported power supply configuration will not provide power supply redundancy and results in the system generating multiple errors to the system event log.

In a redundant power supply 3+1 configuration, 4 pcs power supplies must be powered. If only 3 pcs (or less) power cord are connected to any 3 (or less) of the 4 pcs power supplies, all the CRPS System Status LED will illuminate solid amber when power-up, denoting that a critical system event has occurred.

3.1.1 Three Power Supply (CRPS 3+0) Power Configuration

Platform management will set the system power configuration to CRPS 3+0 configuration (non-Redundant power configuration) with ONLY AC 220V input when it detects that the system has only 3 pcs power supply installed.

With a single functional power supply, the system has no power redundancy and the total available power to the system is limited to the maximum power capacity of the power supply. Should the system power draw exceed the power limits of the power supply, server management will enable throttling which limits I/O operations to system processors, GPU, or both. System performance is impacted until server management restores I/O operations to normal levels. Should the system power draw exceed the power limits of the power supply with throttling enabled, then server management will shut down the system.

A power supply event that shuts down the system generates multiple events and errors that are registered into the system event log (SEL). The state of the System Status LED, front of the I/O board on the front side, changes to solid amber, denoting that a critical system event has occurred.

3.1.2 Four Power Supply (CRPS 3+1) Power Configuration

Platform management will set the system power configuration to CRPS 3+1 configuration (Redundant Power) with ONLY AC 220V input if it detects 4 pcs functional power supplies. In a redundant power configuration, if one power supply fails, the backup power supply will automatically engage and provide the necessary power to maintain optimal system operation.

With 1 pcs power supply failure, the BMC generates several events that are registered to the system event log (SEL) and changes the system power configuration to 3 + 0 (non-redundant) (see section 3.1.1) until the failed power supply is replaced. In addition, the System Status LED, I/O board on the rear side, will change to solid on amber, denoting a degraded but operational system state.

Power supplies are hot-replaceable, allowing a failed power supply to be replaced without having power down the system. After replacing a failed power supply, platform management will automatically change the power configuration to 3+1. The System Status LED state changes back to off, denoting the system is operating in a fault free normal state.

3.2 Closed Loop System Throttling (CLST)

Closed Loop System Throttling (CLST) is supported. CLST prevents the system from crashing if a power supply module overloads or overheats. If the system power reaches a pre-programmed power limit, CLST throttles system memory and/or processors to reduce power. System performance is degraded if throttling occurs.

3.3 Smart Ride Through (SmaRT) Throttling

Smart Ride Through (SmaRT) throttling is supported. SmaRT increases the reliability of a system operating in a heavy power load condition and remains operational during an AC line dropout event.

When AC voltage is too low, a fast AC loss detection circuit inside each installed power supply asserts an SMBALERT# signal to initiate a throttle condition in the system. System throttling reduces the bandwidth to both system memory and processors that, in turn, reduces the power load during the AC line drop out event.

3.4 Current Load Sharing in CRPS

Enable Current Load Sharing in CRPS can Prevent Overloading: Without load sharing, one power module might try to deliver most, or all the current demanded by the load, pushing it beyond its rated capacity and causing it to fail or shut down.

Improves Thermal Management: Operating modules load distribution prevents individual modules from overheating due to excessive current.

Key Characteristics of Current Load Sharing in CRPS:

Accuracy: CRPS specifications define how closely the modules must share the load (e.g., within $\pm 5\%$ or $\pm 10\%$ of the average current). High accuracy is crucial for reliability.

Dynamic Response: The system must quickly rebalance the load if the total system load changes or if a module fails/is removed (or called hot swap).

Fault Tolerance: The sharing mechanism should remain stable even if one module malfunctions.

Benefits of Current Load Sharing in CRPS:

Increased System Reliability: Prevents single-module overloads and ensures smooth failover.

Better Thermal Performance: Heat is spread evenly across modules and the system chassis.

Scalability: Simplifies adding modules to increase capacity, knowing they will share automatically.

3.5 Power Supply Module Efficiency

Each power supply option is rated to meet specific power efficiency limits based on their 80 PLUS power efficiency rating: Titanium.

The following table defines the required minimum power efficiency levels based on their 80 PLUS efficiency rating at specified power load conditions: 100%, 50%, 20%, and 10%.

The AC power supply efficiency is tested over an AC input voltage range of 180–264 Vac (rated 200–240 Vac) without any AC power supply fan.

Table 21. 3200W AC Power Supply Option Efficiency (80 PLUS Titanium)

	Loading	100% of Maximum	50% of Maximum	20% of Maximum	10% of Maximum
	Minimum Efficiency	91%	96%	94%	90%

3.6 AC Power Cord Specifications

You are advised to use the AC power cords that are shipped with the server system. Otherwise, the AC power cord used must meet the specification requirements listed below:

Table 22. AC Power Cord Specifications

Item	Description
Power Cord	C19 type
Cable Type	SJT
Wire Size	14 AWG
Temperature Rating	70°C
Amperage Rating	16A at 250 V
Voltage Rating	250 VAC

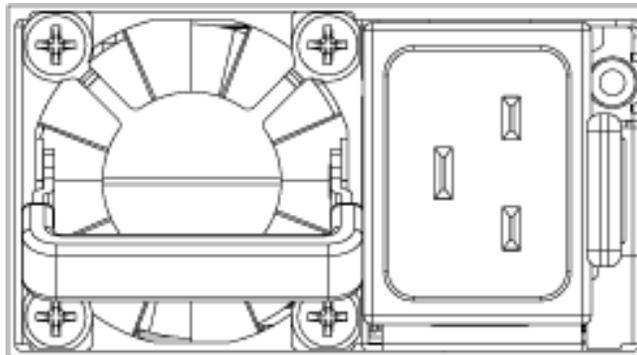


Figure 11. AC Power Cable Connector

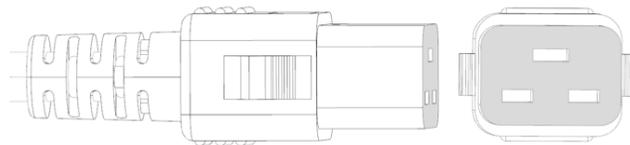


Figure 12. AC Power Cord Outline (C19 Type)

3.7 AC Power Supply Features

3.7.1 Protection Circuits

Each installed power supply module includes several protection circuits that shut down the power supply if a defined operating threshold is exceeded.

3.7.1.1 Over Current / Voltage Protection

Each power supply installed is protected against excess current. The power supply unit shuts down for a specific time period after crossing current thresholds. A power supply that is shut down due to an exceeded protection circuit threshold can be reset by removing source power for 15 seconds.

The AC power cord used must meet the specification requirements listed in the following table.

Table 23. Over Voltage Protection (OVP) Limits

Output Voltage	Minimum (V)	Maximum (V)
+12 V	13.5	14.5

3.7.1.2 Over Temperature Protection (OTP)

Each installed power supply is protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. The power supply unit shuts down during OTP conditions. Once the power supply temperature drops to within specified limits, the power supply restores power automatically.

Chapter 4 High Speed Backplane (HSBP) Overview

The front drive bay of the server system supports up to 8 pcs NVMe drives. The E1.S NVMe High Speed Backplane supports the following features:

- Up to 128 Gb/s E1.S NVMe support
- Hot-swap drive support
- Cable connectors
- LEDs to indicate drive activity and status for each attached device
- Device presence detects inputs to the microcontroller
- 5V voltage regulator (VR) for devices
- 3.3V voltage regulator (VR) for microcontroller
- Microcontroller firmware updateable over the I2C interface
- Field Replaceable Unit (FRU) EEPROM support
- Temperature sensor using a TMP75 (or equivalent) thermistor implementation with the microcontroller

4.1 SGPIO Functionality

Backplanes include support for an SFF-8485 compliant SGPIO interface used to activate the status LED. This interface is also monitored by the microcontroller for changing values of FAULT, IDENTIFY, and REBUILD registers. These items, in turn, are monitored by the HPM board BMC to generate corresponding System Event Log (SEL) events.

4.2 I2C Functionality

The microcontroller has a host/target I2C connection to the HPM board BMC. The microcontroller is not an Intelligent Platform Management Bus (IPMB) compliant device. The BMC generates SEL events by monitoring registers on the HSBP microcontroller for DRIVE PRESENCE, FAULT, and RAID REBUILD in progress.

Table 24. Partial I2C Pinout in a Standard MCIO Connector

Pin #	Signal Name
A9	MCIO_SDA[x]
B26	VPP[x]_SMB_SDA
A8	MCIO_SCL[x]
B27	VPP[x]_SMB_SCL
B9	FM_SMB_PEHP_ALERT[x]_N

Chapter 5 Thermal Management

The embedded platform management subsystem is responsible for keeping the system operating reliably and with the best performance. The integrated baseboard management controller (BMC) embedded within the Aspeed® AST2600 Advanced PCIe® Graphics and Remote Management processor is the most responsible component for determining and implementing system actions under varying environmental and operational conditions.

Thermal management is critical to system performance and long-term reliability. The system is designed to operate at external ambient air temperatures ranging from 10 °C to 35 °C in AS400-2A1-H200-NVL SKU and from 10 °C to 30 °C in AS400-2A1-RTX_PRO_6000 SKU. The system must maintain steady airflow through the system to expel all hot air generated within it.

The system uses ten chassis fans with two rotors in each fan, and an embedded fan within each power supply unit. Cool air is drawn in from the front, directed across several high heat-generating components inside the chassis, and then exhausted through the rear. This airflow design helps dissipate heat efficiently and prevents components from overheating, ensuring the system operates at optimal performance.

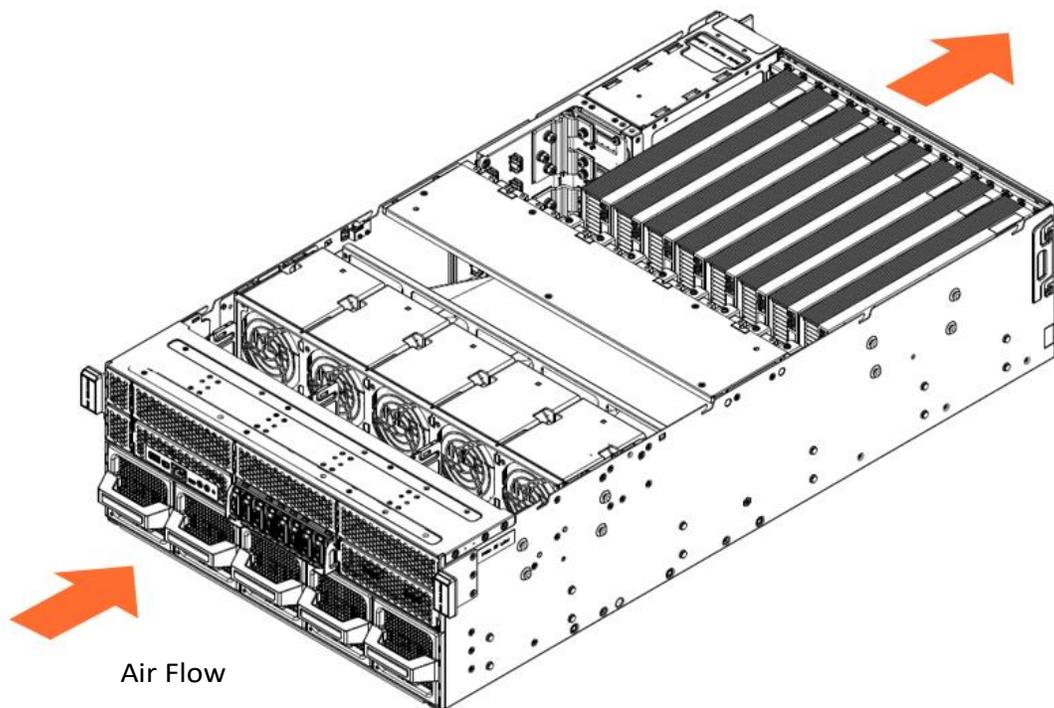


Figure 13. System Air Flow

5.1 Single Rotor Fan Fail Redundancy

The system does not support full fan redundancy. It provides single rotor fail redundancy only in the ACPI S0 power state.

5.2 Thermal Operation and Configuration Requirements

Chassis design and several system components within the system are designed to provide the system with the appropriate air flow necessary to keep the system operating with the best performance. These include:

- Four manageable system fans (80 mm in length, 80 mm in width) (8080 fan)
- Fans integrated into each installed power supply module
- Air duct
- Appropriate processor heatsinks
- Populated drive carriers/rails
- Populated memory slots
- Proper cable route
- System performance may be impacted when operating within the extended operating temperature range.

Note:

All system fans are controlled independently of each other. The fan control system may adjust fan speeds for different fans based on increasing/decreasing temperatures in different thermal zones within the chassis.

▼ Fan0_Front	16050 Rpm
▼ Fan0_Rear	16200 Rpm
▼ Fan1_Front	16050 Rpm
▼ Fan1_Rear	16350 Rpm
▼ Fan2_Front	16050 Rpm
▼ Fan2_Rear	16200 Rpm
▼ Fan3_Front	15750 Rpm
▼ Fan3_Rear	16050 Rpm

Figure 14. Example of Dual Rotor Fan Information in BMC WebUI “Sensor” Submenu

If system temperatures continue to rise while the system fans are operating at maximum speed, the platform management may throttle the I/O bandwidth of the processors, GPU, or both of them. This mechanism prevents components from overheating and helps keep the system operational. Throttling continues until system temperatures drop below the predefined thermal thresholds.

If system temperatures exceed the maximum thermal limits, the system automatically shuts down. The status LED in front side turns solid amber, and the event is recorded in the system event log.

The power supply unit (PSU) includes protection against over-temperature conditions caused by excessive ambient temperatures. When such a condition occurs, the PSU automatically shuts down to prevent damage. If the temperature inside the PSU exceeds its maximum thermal limit, or if the PSU fan fails, the PSU will shut down to protect itself.

5.3 System Fans

Ten 80 mm (W), 80 mm (D), 80 mm (H) system fans and an embedded fan for each installed power supply module provide the primary airflow for the system. All four system fans are mounted within a single fan assembly module that can be removed for cable routing or to service other components within the chassis.

Each system fan supports the following:

- Toolless replacement
- Designed for tool-less insertion and extraction from the fan assembly.
- Featuring a tachometer signal that allows the integrated BMC to monitor its status.
- Fan speed is controlled by integrated platform management. As system thermals fluctuate high and low, the integrated BMC firmware increases and decreases the speeds to specific fans within the fan assembly to regulate system thermals.
- Integrated fault status LED. Platform management illuminates the (fault) status LED to solid amber on for the failed fan.

5.4 Power Supply Module Fans

Each installed power supply module includes an embedded (non-removable) 40 x 40 x 40 mm fan. This fan is responsible for airflow through the power supply module and is managed by the fan control system.

The power supply will send Alert_N signal [fan in power supply fail or OTW (Over Temperature Warning) and so on] to the system if the temperature of thermal sensors in the power supply over 62°C; and send OTP (Over Temperature Protection) to shut down the power supply if the temperature of thermal sensors in the power supply over 65°C

5.5 Fan Speed Control

The BMC controls and monitors the system fans. Each fan is associated with a fan speed sensor that detects a fan failure. The system fans are divided into fan domains, each of which has a separate fan speed control signal, and a separate configurable fan control policy. A fan domain can have a set of temperature and fan sensors associated with it. The sensors are used to determine the current fan domain state.

A fan domain has three states: sleep, boost, and nominal. The sleep and boost states have fixed (but configurable through OEM SDRs) fan speeds associated with them. The nominal state has a variable speed determined by the fan domain policy. An OEM SDR record is used to configure the fan domain policy.

The fan domain state is controlled by several factors, listed in the following bullets in order of precedence from high to low. If any of these conditions apply, the fans are set to a fixed boost state speed.

- An associated fan is in a critical state or missing. The SDR describes which fan domains are boosted in response to a fan failure or removal in each domain. A fan cannot be detected if it is removed when the system is in fans-off mode.
- Any associated temperature sensor is in a critical state. The SDR describes which temperature-threshold violations cause fan boost for each fan domain.
- The BMC is in a firmware update mode, or the operational firmware is corrupted.

Note:

During a BMC firmware update, the system fans maintain their current rotation speed from the time of the update. Users should avoid adding extra system load during the update process to prevent thermal-related issues that may cause system instability.

Chapter 6 System Hardware Removal and Installation

This chapter provides instructions on removing and installing system components. Except for installing the chassis handle, E1.S drive, and single power supply unit only, the installation or replacement of other components requires that the system be powered off first. Please follow the procedures given in each section.

Note:

Electrostatic Discharge (ESD) can damage electronic components. To prevent such damage to PCBs (printed circuit boards), it is important to use a grounded wrist strap, handle all PCBs by their edges and keep them in anti-static bags when not in use.

Note:

The system images are for demonstration purposes only. The appearance and internal view of your system may vary.

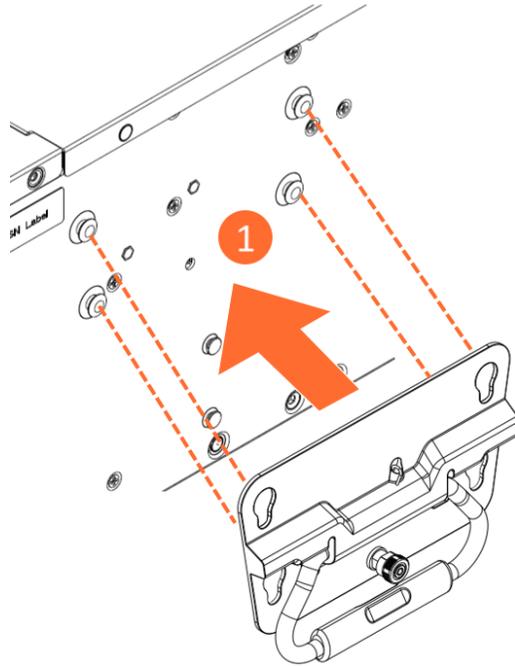
6.1 Chassis Handle

6.1.1 Installing the Chassis Handle

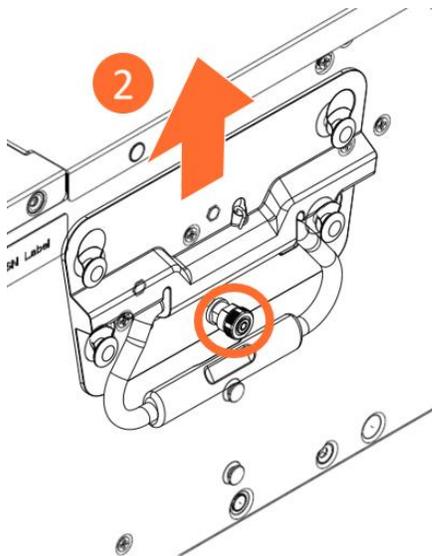
Steps

Follow the instructions below to install four handles to the system to safely carry the system:

1. Align the four openings of the handle with the studs on either side of the chassis and then insert the handle into the system.



2. Pull the handle upward until the spring-loaded plunger engages in the hole.



3. Repeat steps 1 to 2 to install the remaining three handles to the system.

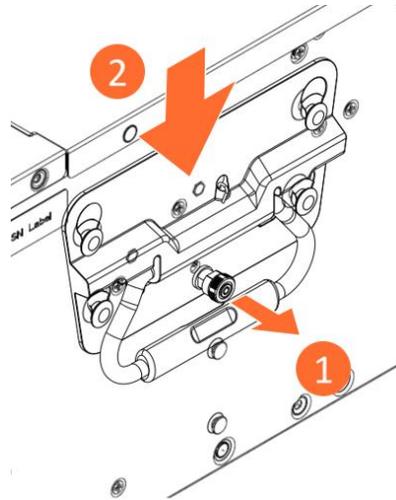
6.1.2 Removing the Chassis Handle

Note:

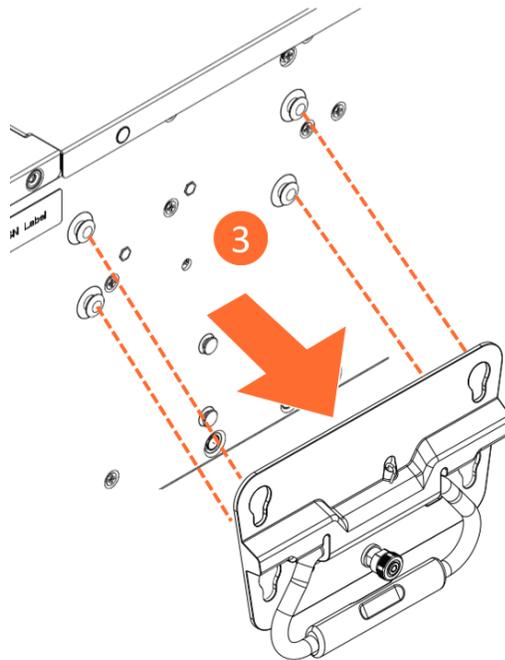
The handles MUST be removed before installing the system into a rack.

Steps

1. Pull the plunger outward to unlock the handle.
2. Pull the handle downward to detach it from the chassis.



3. Remove the handle from the chassis.



4. Repeat steps 1 to 3 to remove the remaining three handles from the system.

6.2 Hard Drive

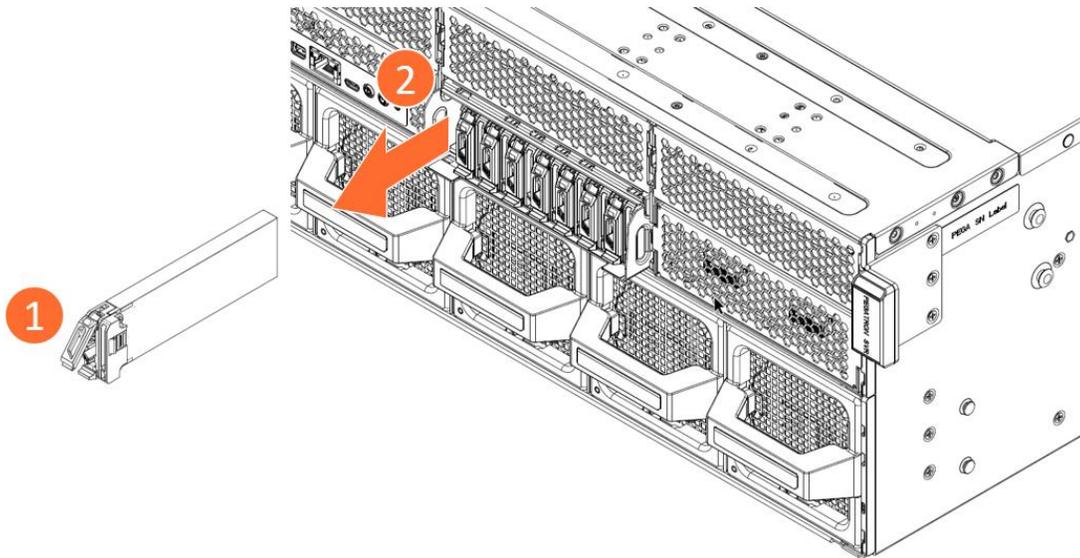
Note:

You are advised to install the E1.S drives starting from the most left slot to the right (front view of the server) in the sequence of slot #0 > #1 > #2 > #3 > #4 > #5 > #6 > #7.

6.2.1 Removing the Hard Device Assembly

Steps

1. Press the latch on the front side of the hard drive assembly to unlock the lever.
2. Pull out the lever to pull the assembly out of the system.



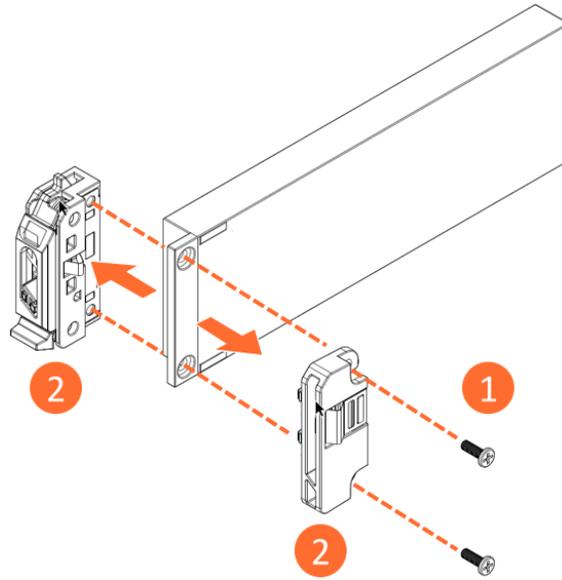
6.2.2 Removing the Dummy

The hard drive assembly is pre-installed with a dummy. Follow the steps below to remove the dummy before installing a drive:

1. Remove the two M2 size screws securing the drive cover to the drive base and then remove the cover.
2. Remove the drive cover and drive base from the dummy.

Note:

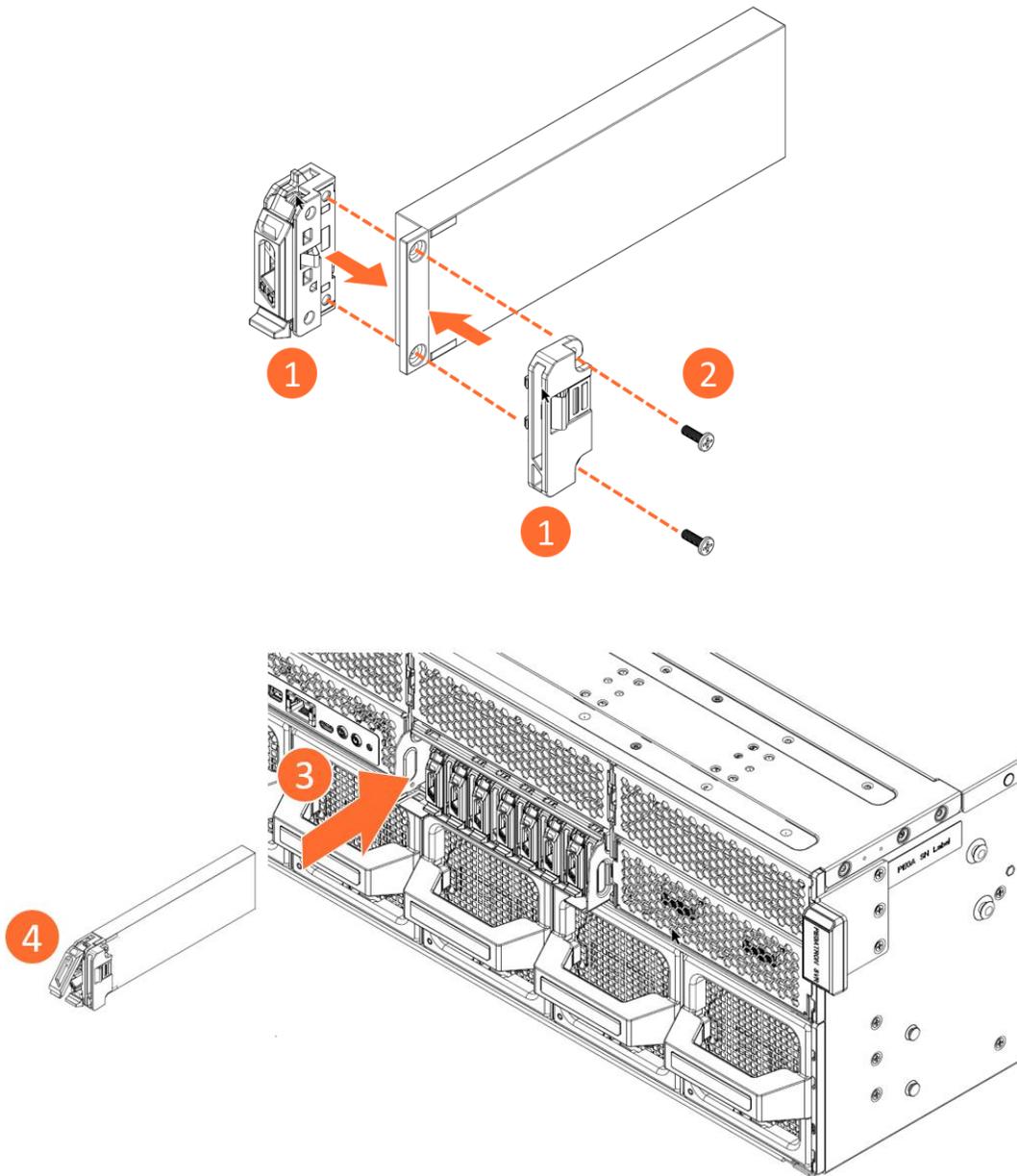
For optimistic thermal effects, the drive slot MUST be installed with either a hard drive or a dummy. Install the dummy back to the system if a drive slot is not occupied with a drive.



6.2.3 Installing the Hard Device

Steps

1. Install the hard drive to the drive base and the drive cover to the drive.
2. Install two M2 size screws to bundle the cover, drive, and base together as an assembly (torque: 2 ± 0.2 kgf-cm).
3. Install the drive assembly into the system.
4. Push down the lever to lock the assembly in place.



6.3 Power Supply Unit

The power supply unit (PSU) is hot-swappable. However, if you need to replace more than two PSUs, replace one unit after another. DO NOT remove more than two PSUs at a time when the system is powered on or the CPU will enter throttling mode, GPU will enter power brake mode, and the system performance will be compromised.

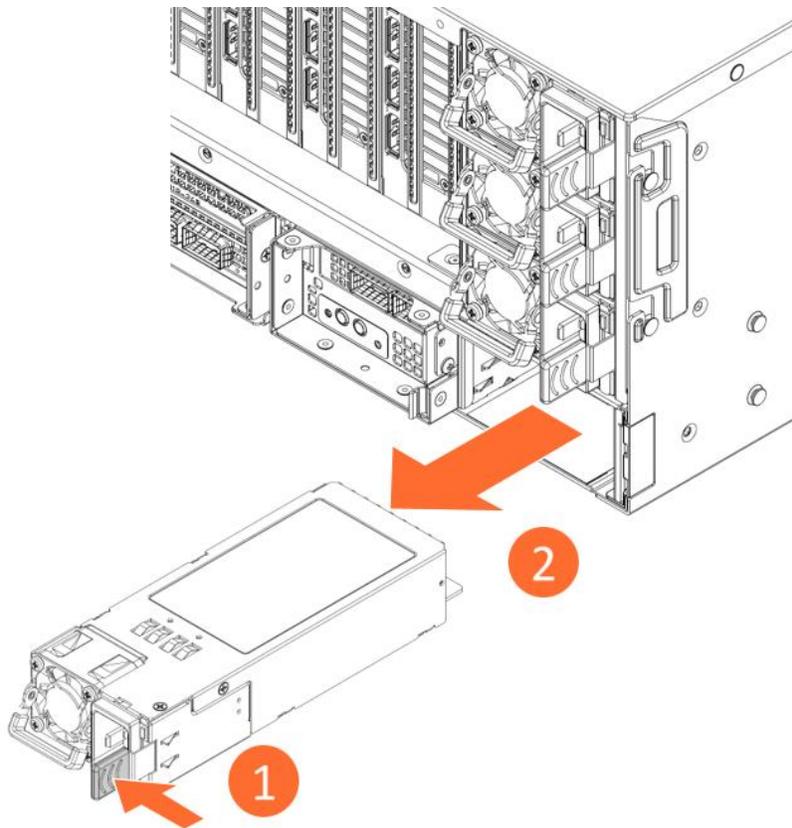
6.3.1 Removing the Power Supply Unit

Prerequisites

1. Disconnect the power cord from the power supply unit that you want to remove.

Steps

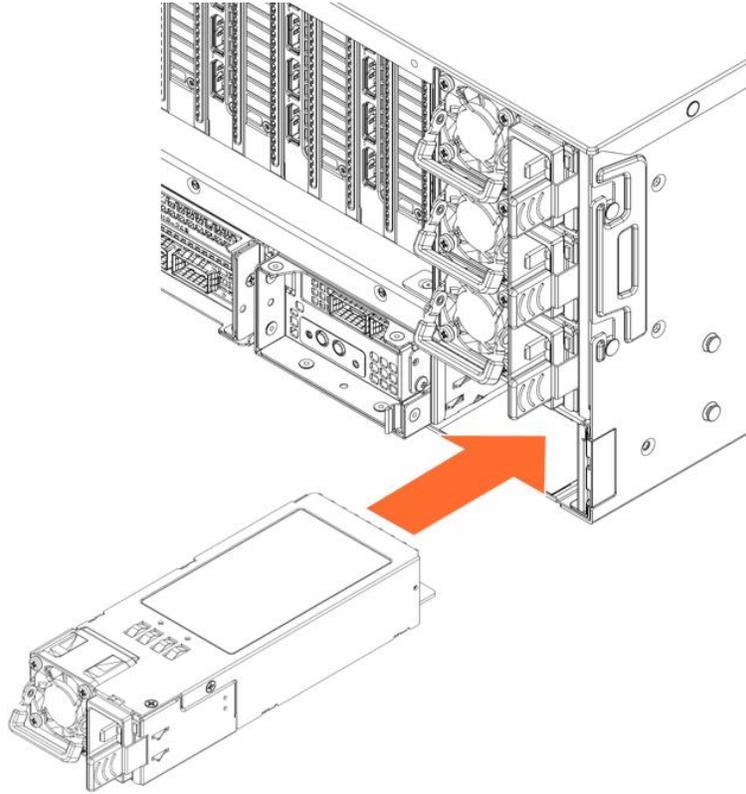
1. Grasp the handle of the power supply unit while pushing its locking tab to its left side.
2. Pull out the power supply unit to remove it from the system.



6.3.2 Installing the Power Supply Unit

Steps

1. Slide the power supply unit into the slot and ensure it clicks into place.



6.4 Front Fan

Note:

The front fan is NOT hot-swappable. The system MUST be powered off before removing/installing a front fan.

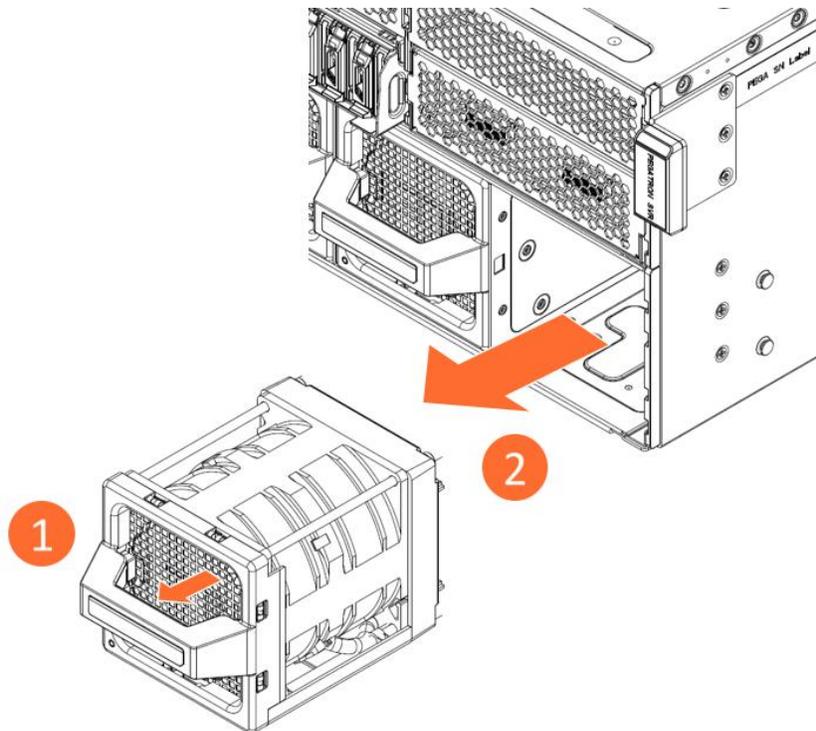
6.4.1 Removing the Front Fan

Prerequisites

1. DC power off the system.

Steps

2. Press and hold the inside of the fan handle to release the fan latch.
3. Pull the fan out of the system.



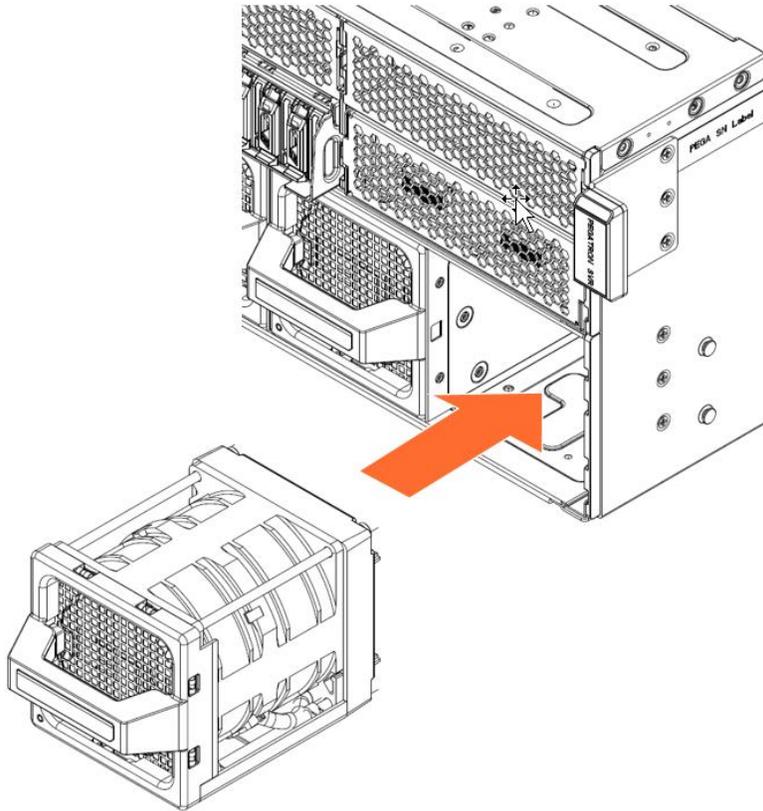
6.4.2 Installing the Front Fan

Prerequisites

1. DC power off the system.

Steps

1. Insert the fan into the slot and ensure it is well seated.



6.5 Top Cover

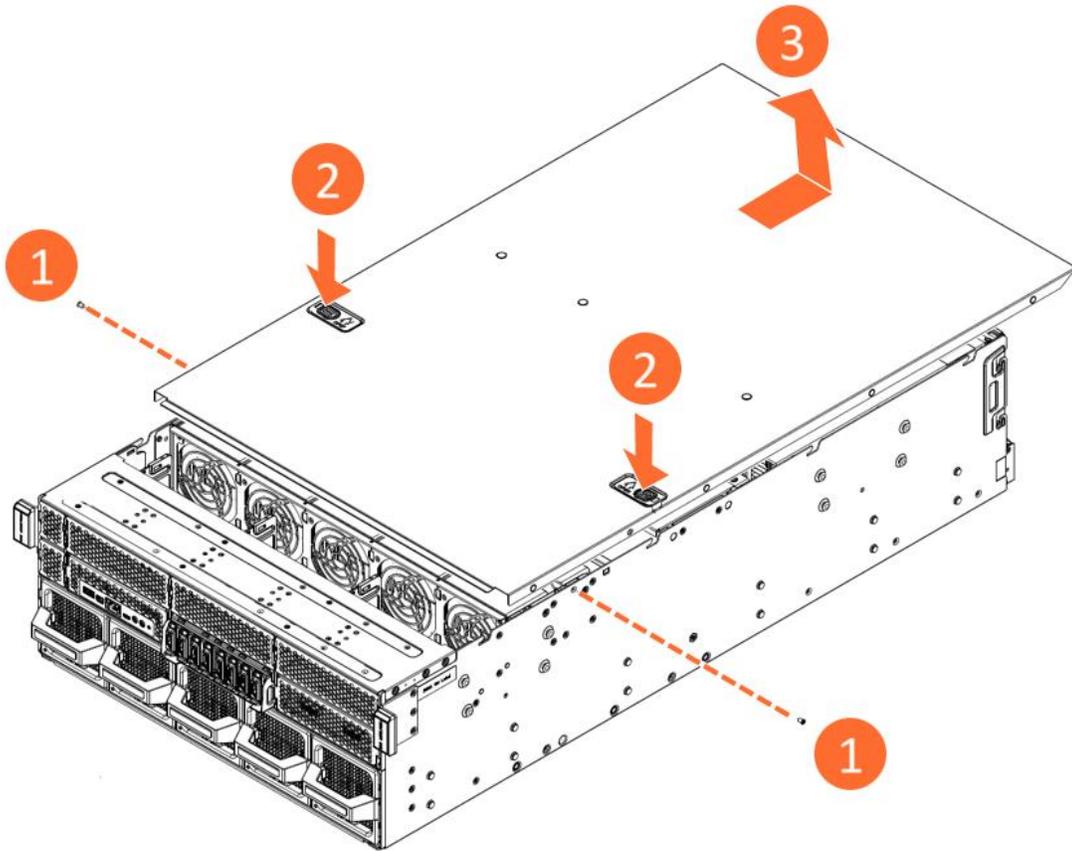
6.5.1 Removing the Top Cover

Prerequisites

1. AC power off the system.

Steps

1. Remove the two #6-32 screws securing the top cover in place.
2. Using your hands, press the latches on the sides of the cover.
3. Push the cover to the rear of the system and then lift it up to remove it from the system.



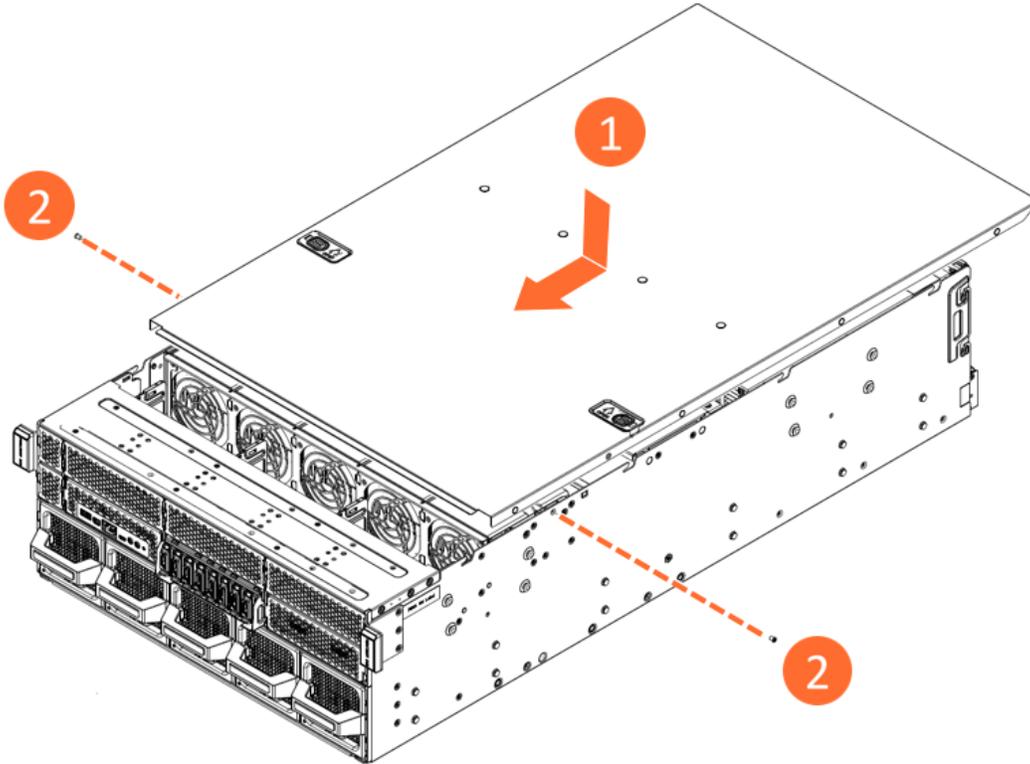
6.5.2 Installing the Top Cover

Prerequisites

1. AC power off the system.

Steps

1. Place the cover on the system and push the cover to the front side of the system until it is engaged with the system.
2. Install two #6-32 screws to secure the top cover in place (9 ± 0.5 kgf-cm).



6.6 Top Fan

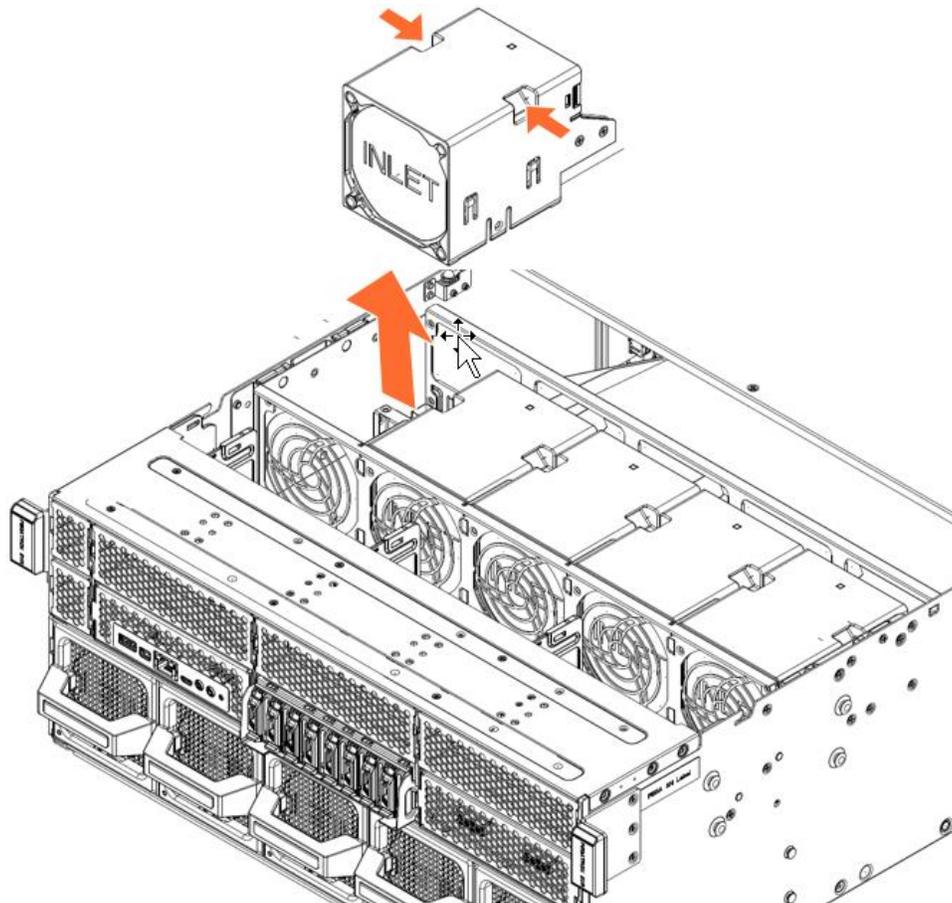
6.6.1 Removing the Top Fan

Prerequisites

1. AC power off the system.
2. Remove the top cover.

Steps

1. Holding the indents on the sides of the fan that you want to remove and then lift it up to remove it from the fan cage.



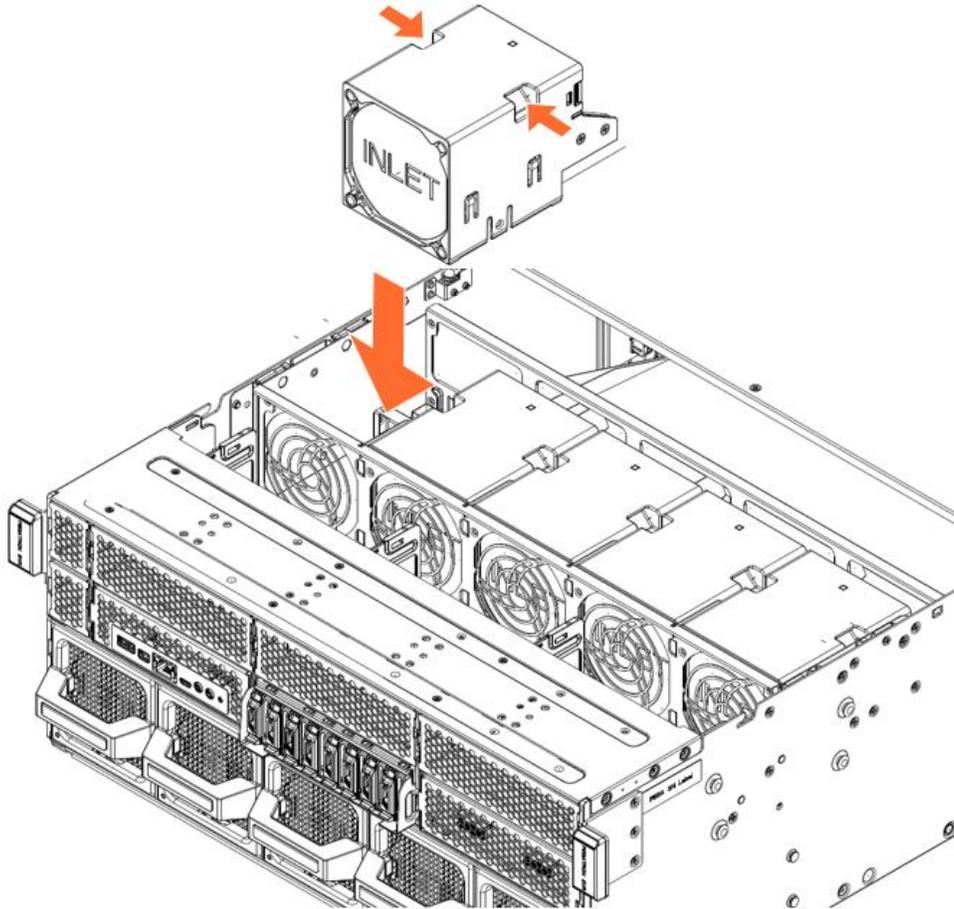
6.6.2 Installing the Top Fan

Prerequisites

1. AC power off the system.
2. Remove the top cover.

Steps

1. Hold the indents on the sides of the fan and then fully insert the fan into the slot until it clicks in place.



6.7 GPU Card

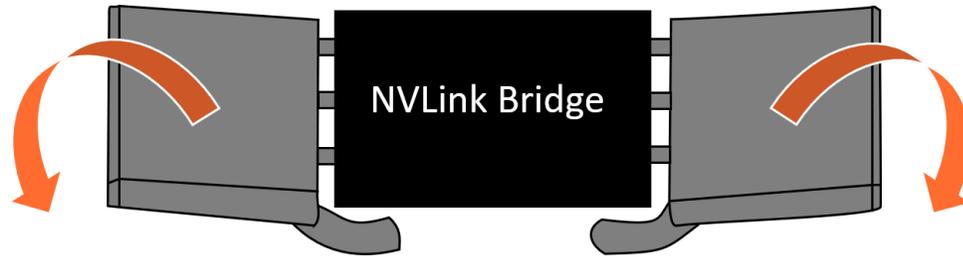
6.7.1 Removing the GPU Card

Prerequisites

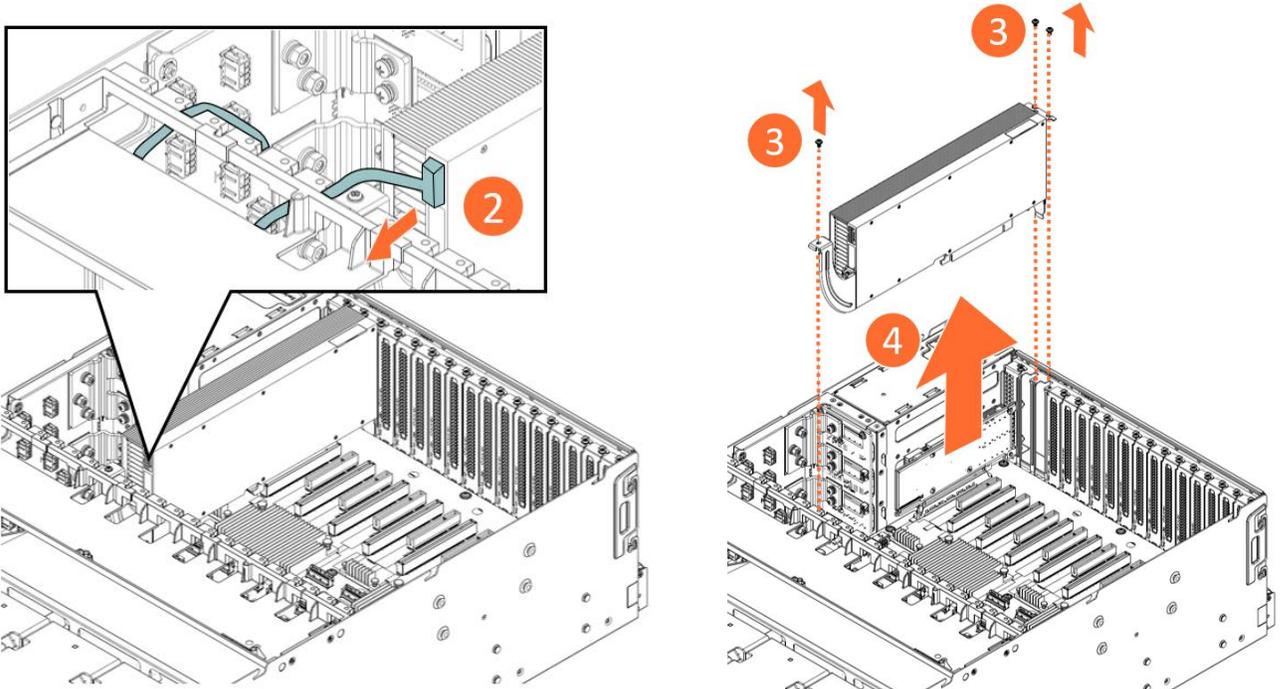
1. AC power off the system.
2. Remove Top Cover.

Steps

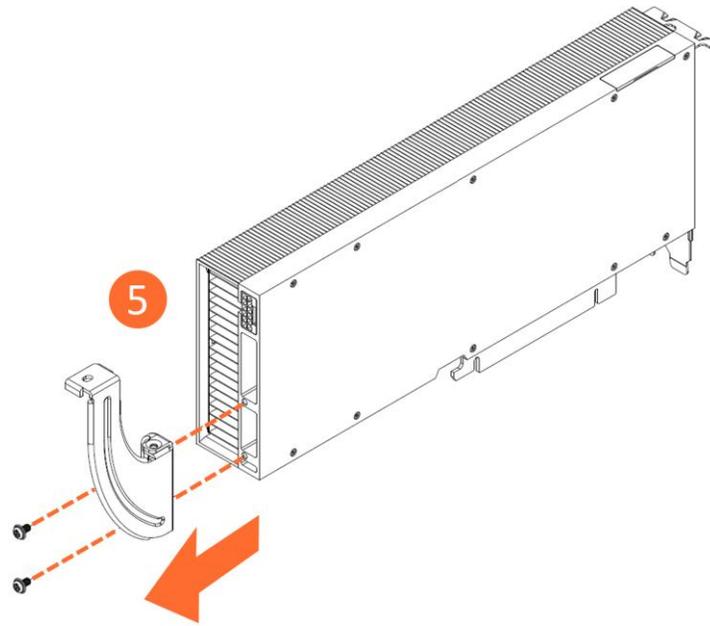
1. [For systems shipped with multiple H200 NVL GPU cards only] Using the removal tools shipped with the system, remove the NVLink Bridge Board(s) from the top side of the GPU cards.



2. Disconnect the GPU card power cable from the GPU card that you want to remove.
3. Remove three M3 screws securing the GPU card assembly in place.
4. Remove the GPU card assembly from the system.



5. Remove two M3 screws securing the GPU card extension bracket to the GPU card and then remove the bracket from the GPU card.



6.7.2 Installing the GPU Card

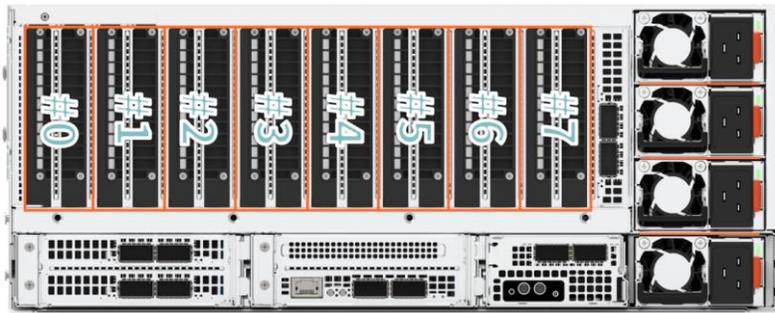


Figure 15. Recommended GPU Card Installation Sequence

Note:

You are advised to install the GPU cards from the right side of the system (at the rear view of the system) in the sequence of #7 > #6 > #5 > #4 > #3 > #2 > #1 > #0.

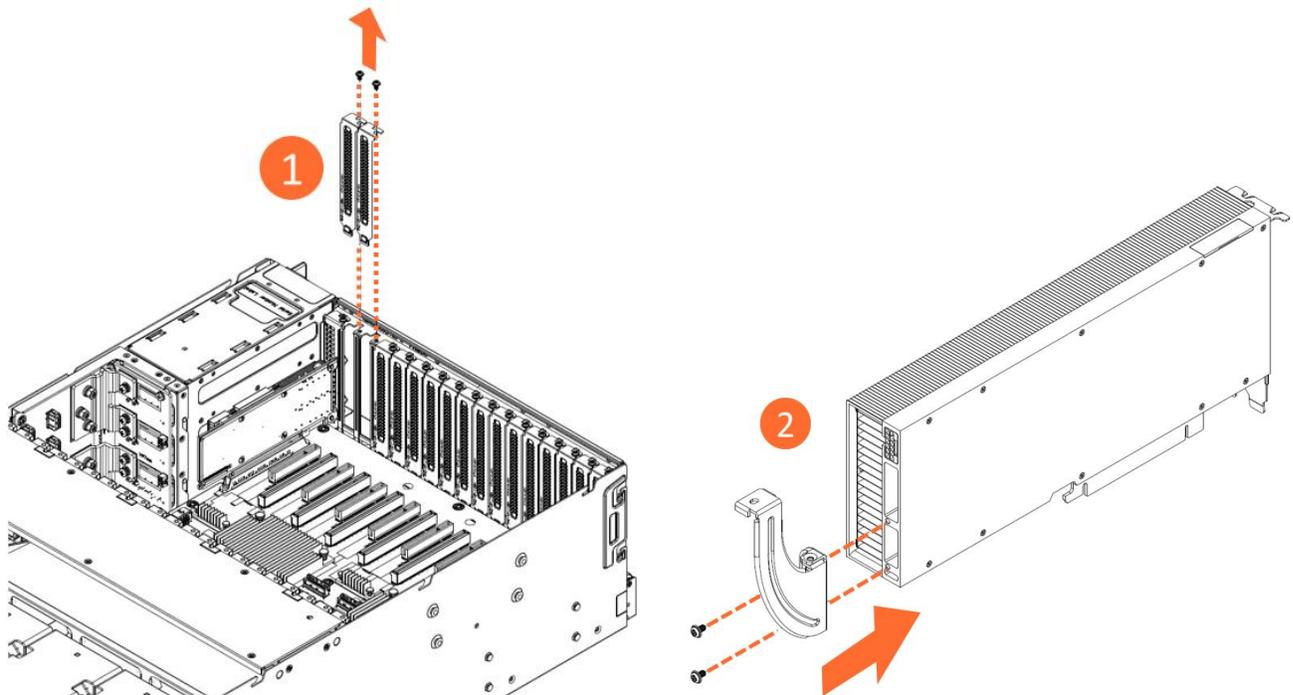
Use the extension brackets shipped with the server system to properly secure the GPU cards in place.

Prerequisites

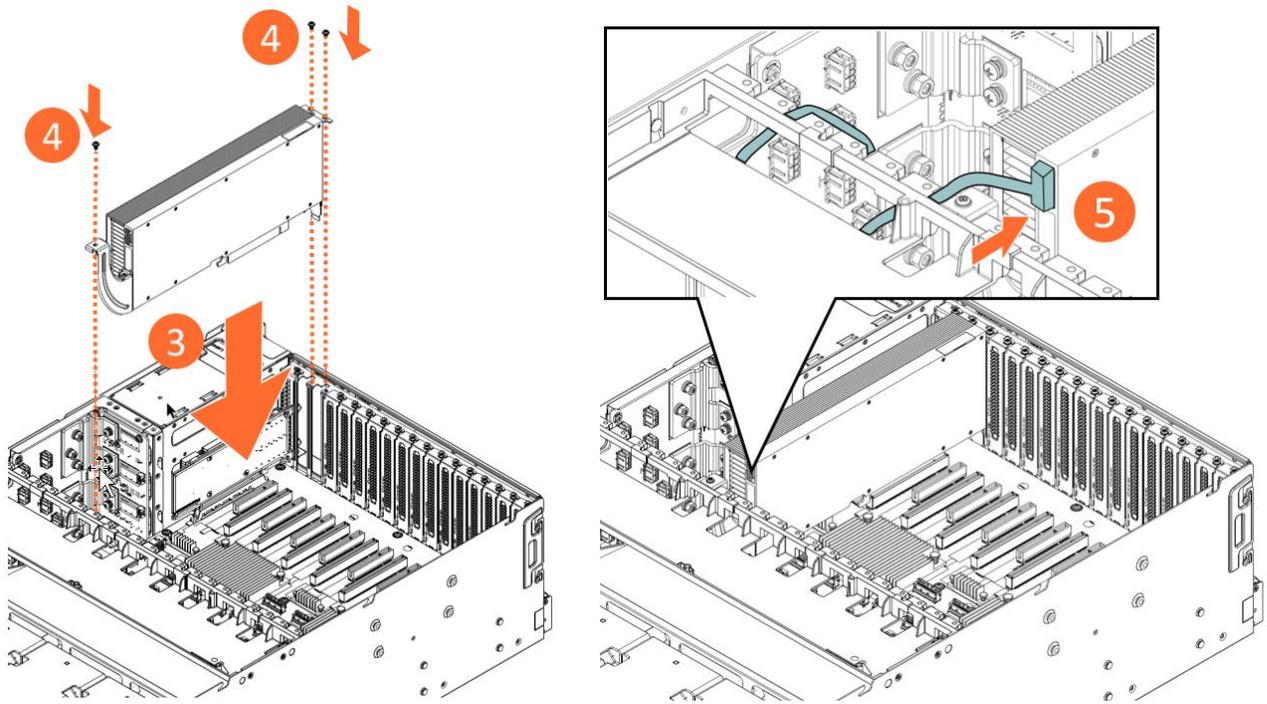
1. AC power off the system.
2. Remove Top Cover.

Steps

1. [For the dual slots that have no GPU card installed] Remove two M3 screws securing two dummy PCIe brackets in place and remove the brackets from the system.
2. Install an extension bracket to the GPU card and then install two M3 screws to secure it in place (6 ± 0.5 kgf-cm).



3. Install the GPU card assembly into the system.
4. Install three M3 screws to secure it in place (6 ± 0.5 kgf-cm).
5. Connect the GPU card cable to the GPU card.



6. [For systems shipped with multiple H200 NVL GPU cards only] Remove the NVLink bridge board cover(s) from the NVLink Bridge Board(s) and then install the bridge board(s) to the top side of the GPU cards.

6.8 GPU Cable Support Bracket

The GPU card power cables are pre-installed into the GPU card support bracket. You are advised to remove and install the cables along with the bracket during any maintenance procedures.

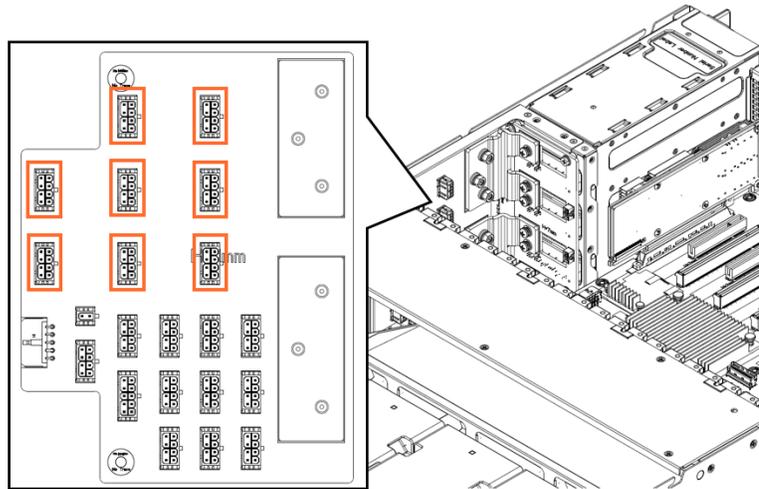
6.8.1 Removing the GPU Cable Support Bracket

Prerequisites

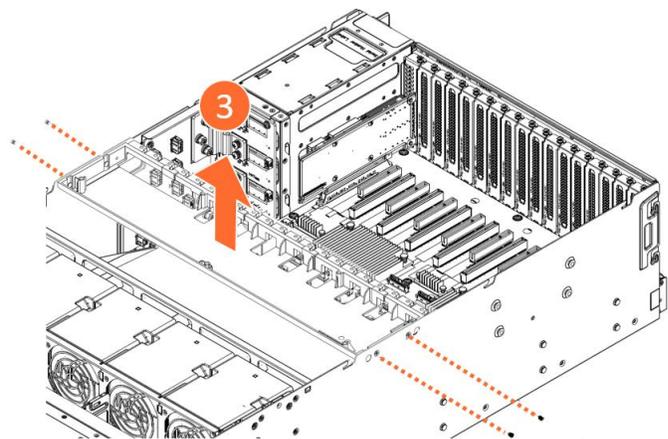
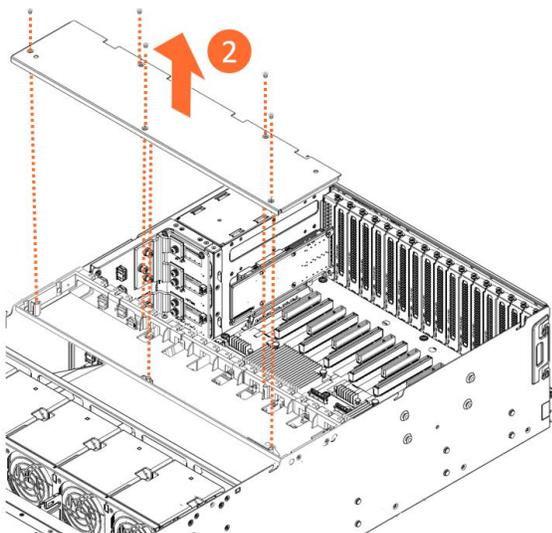
1. AC power off the system.
2. Remove Top Cover and any GPU Card(s).

Steps

1. Disconnect eight GPU card power cables from the #2 power distribution daughter board.



2. Remove five #6-32 screws securing the GPU card support bracket cover in place and then remove the cover.
3. Remove four #6-32 screws securing the GPU card support bracket in place and then remove the bracket with eight GPU card power cables.



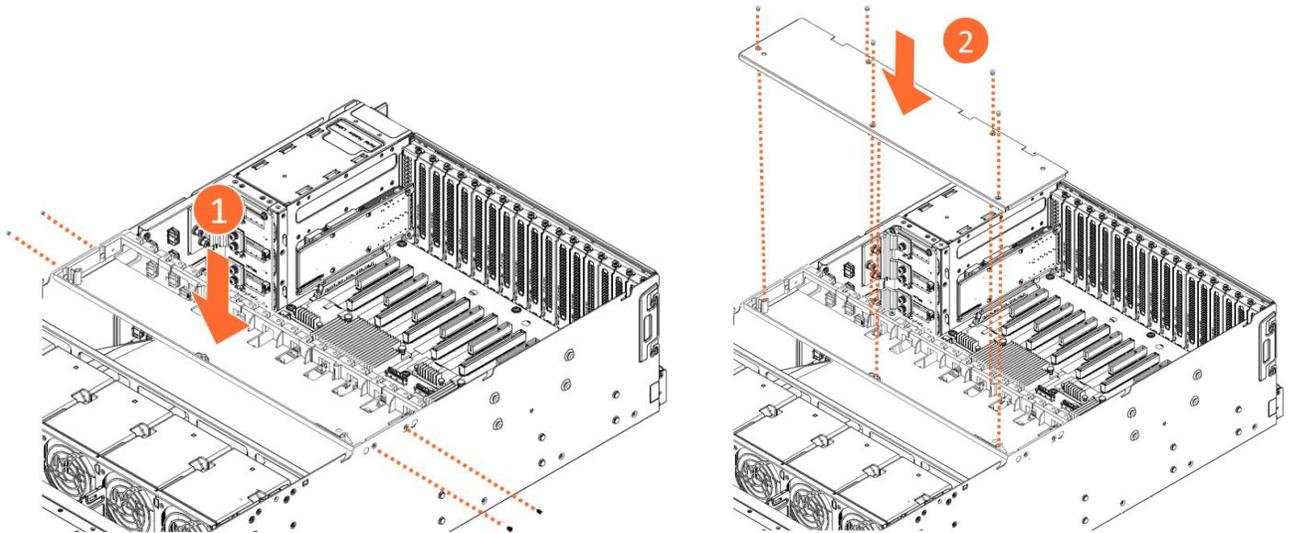
6.8.2 Installing the GPU Cable Support Bracket

Prerequisites

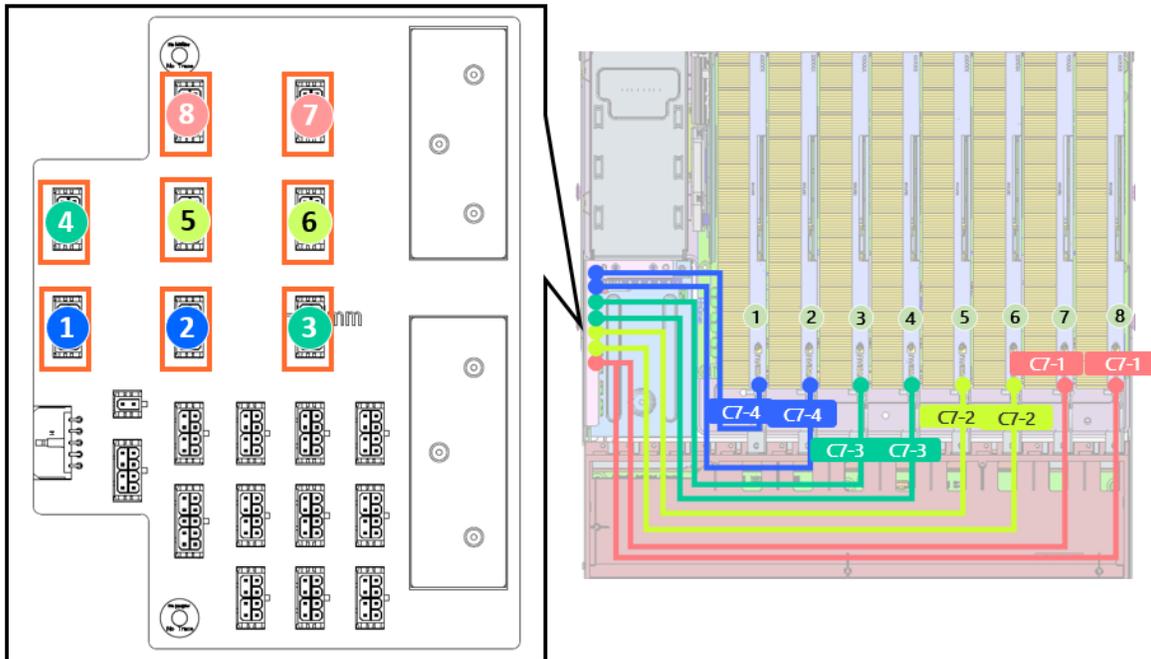
1. AC power off the system.
2. Remove Top Cover and GPU Card.

Steps

1. Install the GPU card support bracket with eight GPU card power cables and then install four #6-32 screws to secure it in place (9 ± 0.5 kgf-cm).
2. Install the GPU card support bracket cover and then install five #6-32 screws to secure it in place (9 ± 0.5 kgf-cm).



3. Connect the eight GPU card power cables to the #2 power distribution daughter board.



6.9 Top Fan Cage Assembly

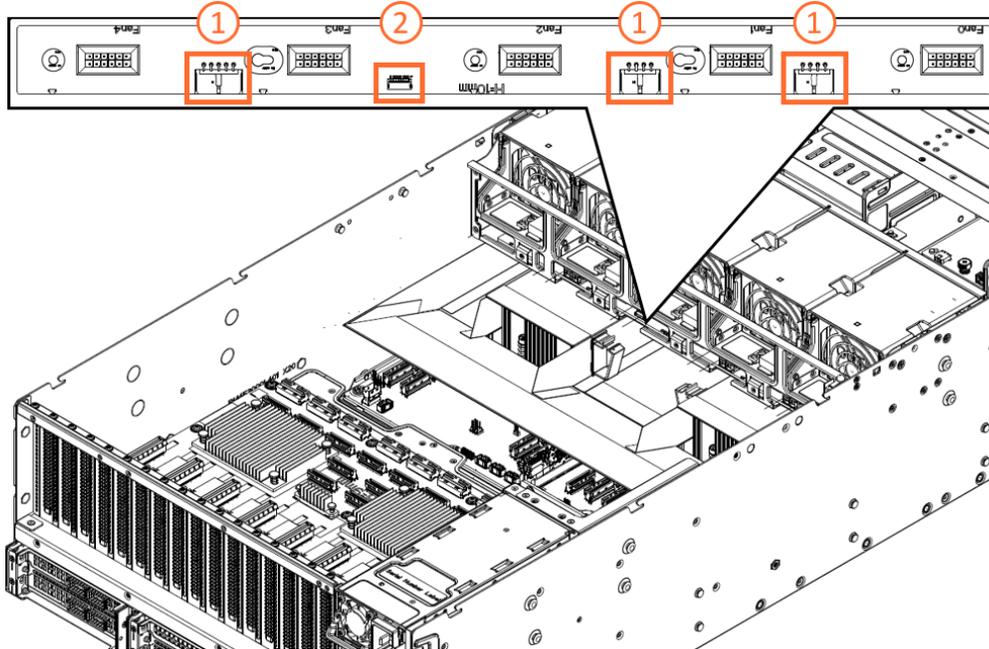
6.9.1 Removing the Top Fan Cage Assembly

Prerequisites

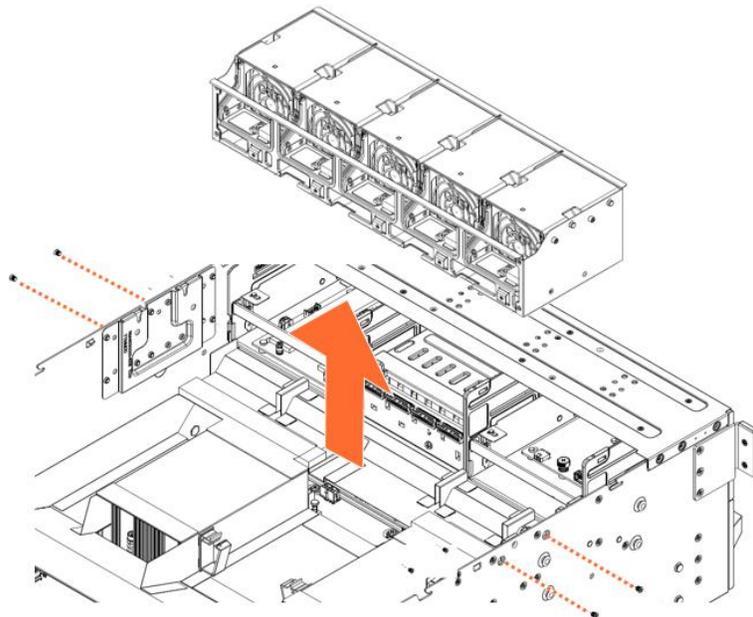
1. AC power off the system.
2. Remove Top Cover, GPU Card, and GPU Card Support Bracket.

Steps

1. Disconnect (1) three power cables and (2) one fan signal cable from the top fan daughter board.



2. Remove four 6-32 screws securing the fan cage in place and remove the fan cage with fans from the system.



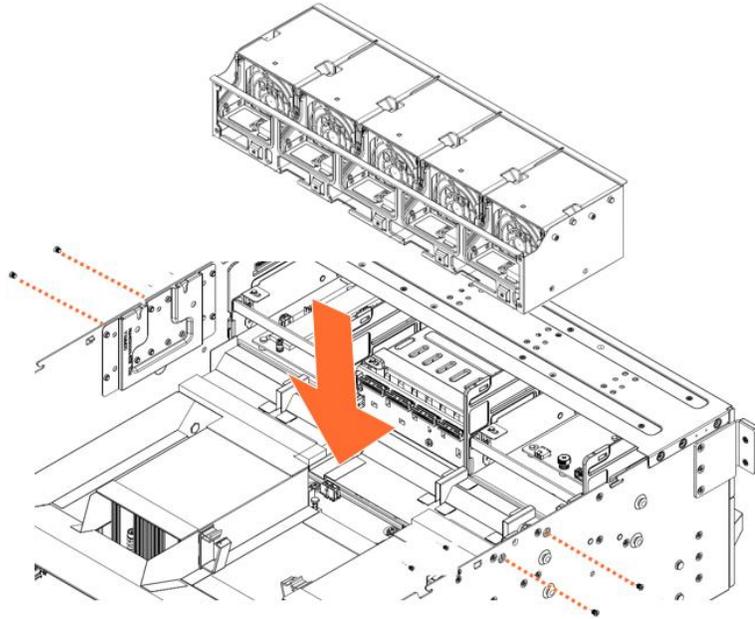
6.9.2 Installing the Top Fan Cage Assembly

Prerequisites

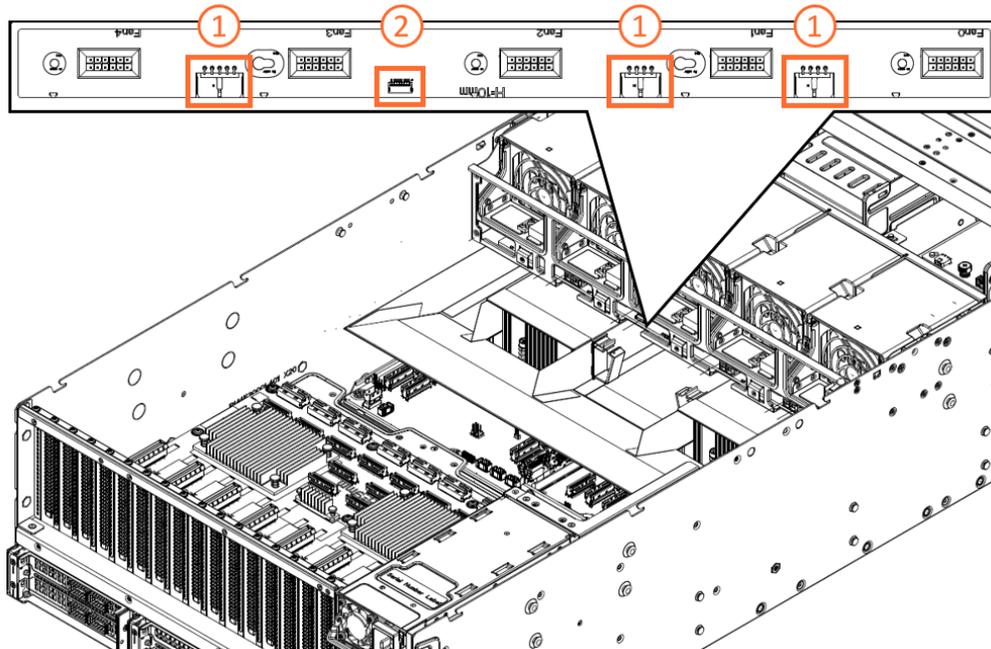
1. AC power off the system.
2. Remove Top Cover, GPU Card, and GPU Card Support Bracket.

Steps

1. Install the fan assembly to the system and then install four 6-32 screws (9±0.5 kgf-cm) to secure it in place.



2. Connect (1) three fan power cables and (2) one fan signal cable to the fan daughter board.



6.10 Air Duct

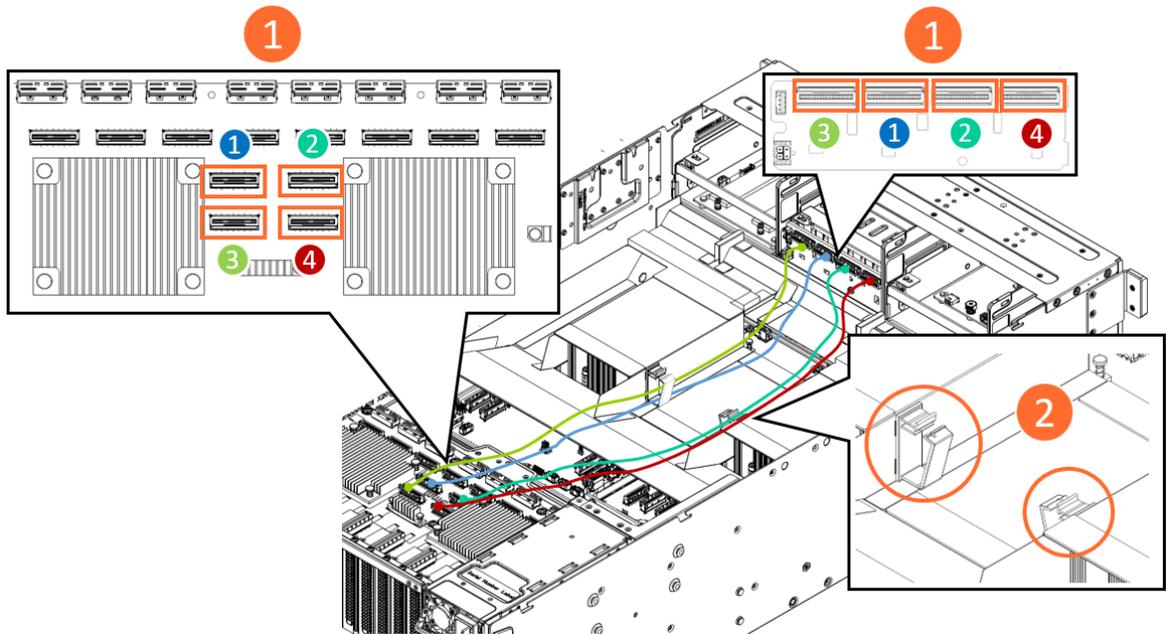
6.10.1 Removing the Air Duct

Prerequisites

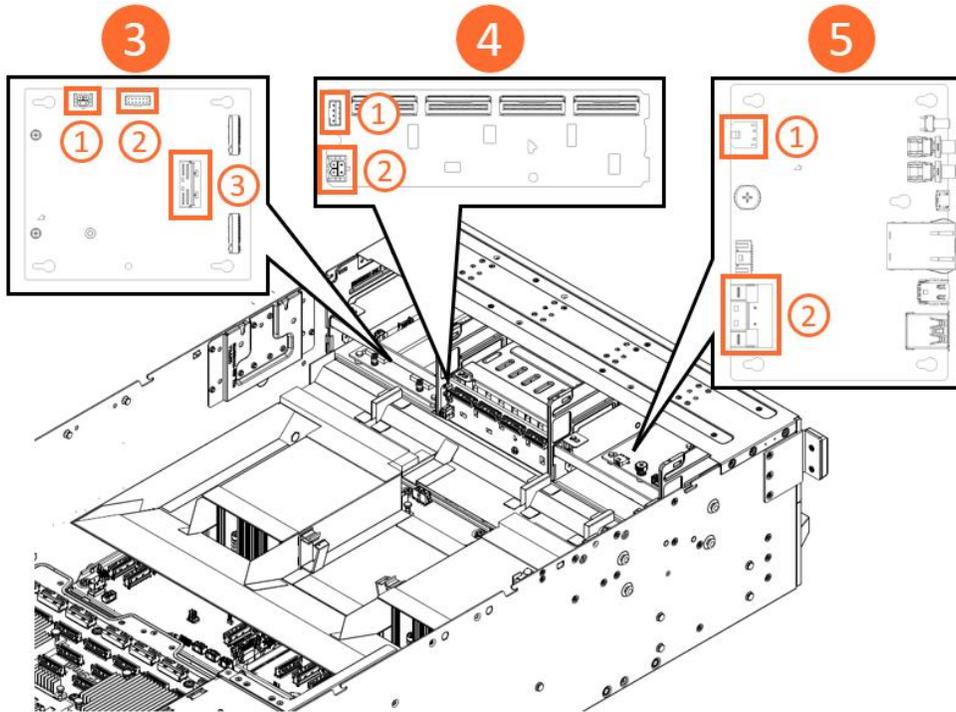
1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, and Top Fan Cage Assembly.

Steps

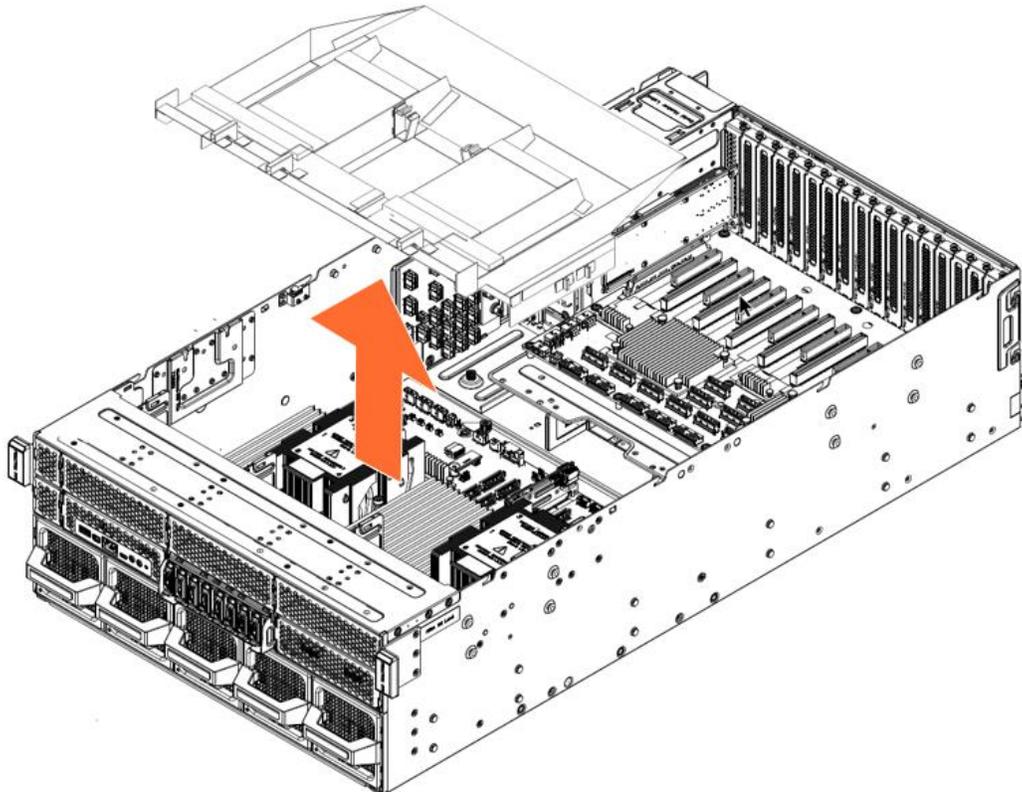
1. Disconnect #1 to #4 E1.S MCIO cables from the E1.S daughter board and switch board.
2. Unthread the #1 to #4 E1.S MCIO cables from the clips on the air duct and then remove the four cables from the system.



3. Disconnect the (1) M.2/E1.S BP power cable, (2) M.2 sideband cable, and (3) M.2 MCIO cable from the M.2 daughter board and then unthread the cables from the air duct.
4. Disconnect the (1) E1.S sideband cable and (2) M.2/E1.S BP power cable from the E1.S backplane daughter board and then unthread the cables from the air duct.
5. Disconnect the (1) front IO power cable and (2) front IO slim SAS cable from the front IO daughter board and then unthread the cables from the air duct.



6. Lift the air duct to remove it from the system.



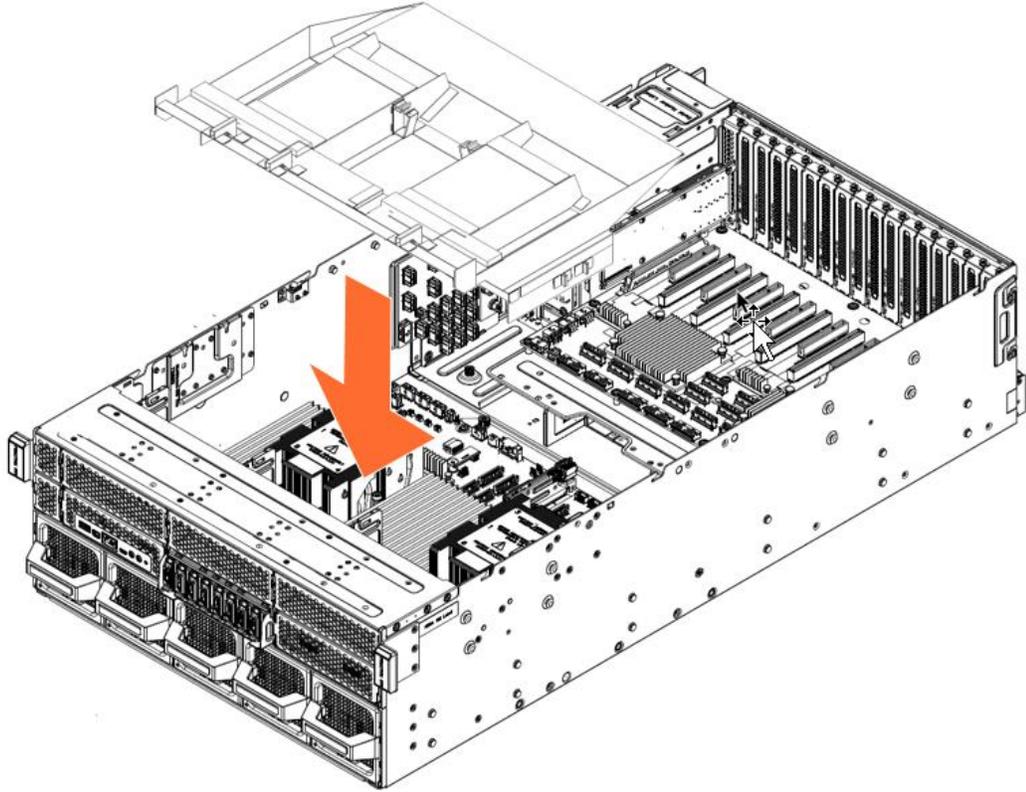
6.10.2 Installing the Air Duct

Prerequisites

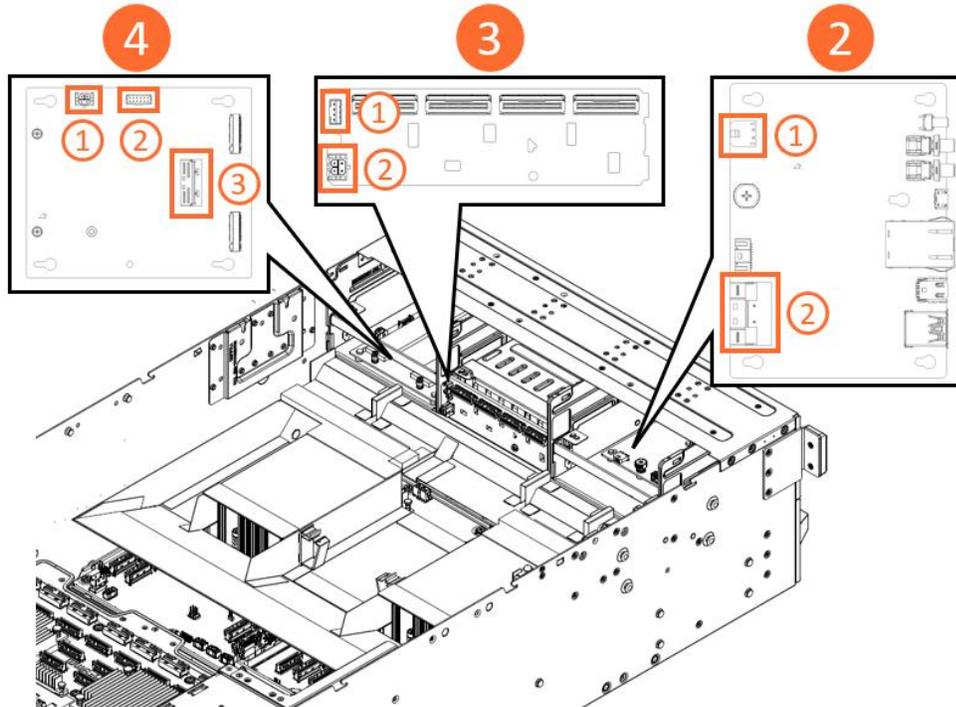
1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, and Top Fan Cage Assembly.

Steps

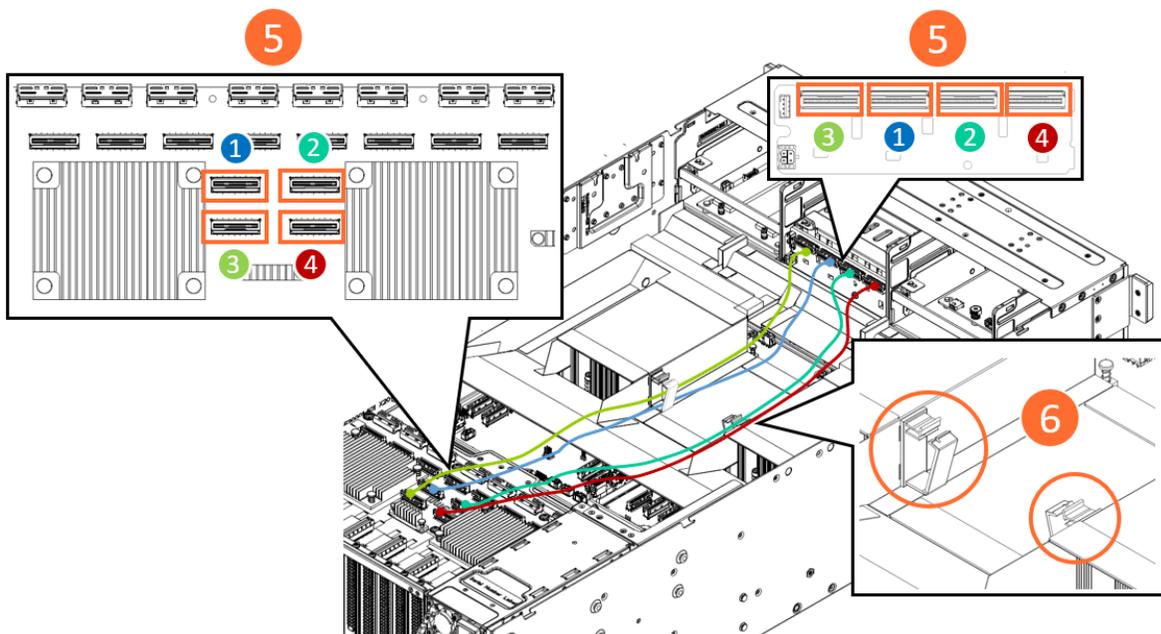
1. Install the air duct back to the system.



2. Connect the (1) front IO power cable and (2) front IO slim SAS cable to the front IO daughter board and then route the cables through the gap between the right side of the air duct and chassis.
3. Connect the (1) E1.S sideband cable and (2) M.2/E1.S BP power cable to the E1.S backplane daughter board and then route the cables through the gap between the right side of the air duct and chassis.
4. Connect the (1) M.2/E1.S BP power cable, (2) M.2 sideband cable, and (3) M.2 MCIO cable and then route the cables through the gap between the left side of the air duct and chassis.



5. Connect #1 to #4 E1.S MCIO cables to the E1.S daughter board and switch board.
6. Route the #1 to #4 E1.S MCIO cables over the air duct and secure the cables in place with two pairs of clips on the air duct.



6.11 M.2 SSD

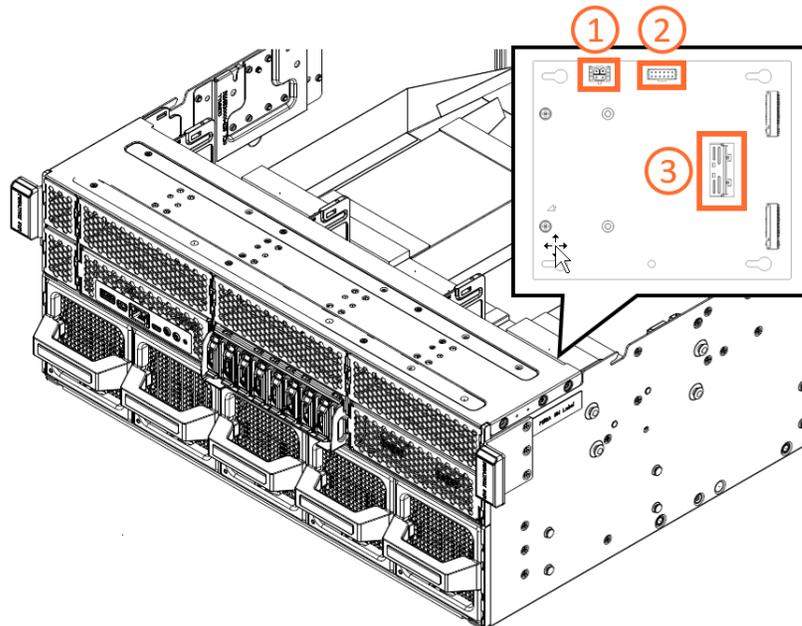
6.11.1 Removing the M.2 SSD Cage

Prerequisites

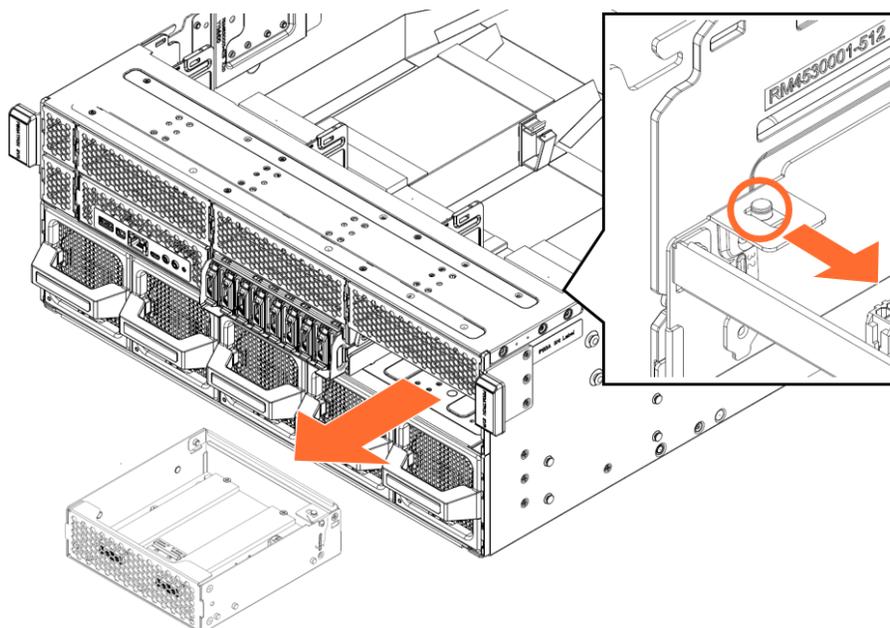
1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, and Top Fan Cage Assembly.

Steps

1. Disconnect the (1) M.2/E1.S BP power cable, (2) M.2 sideband cable, and (3) M.2 MCIO cable from the M.2 daughter board.

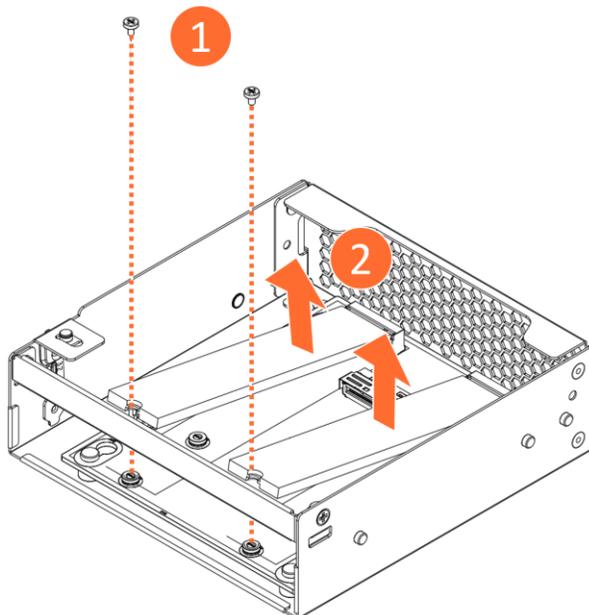


2. Push the latch on top of the M.2 tray toward the center of the chassis to detach it from the system and then pull the tray out of the system.



6.11.2 Removing the M.2 SSD

1. Remove the single M.2 screw securing the M.2 SSD that you want to remove.
2. Remove the M.2 SSD.
3. Repeat steps 1 to 2 if you want to remove the other M.2 SSD.

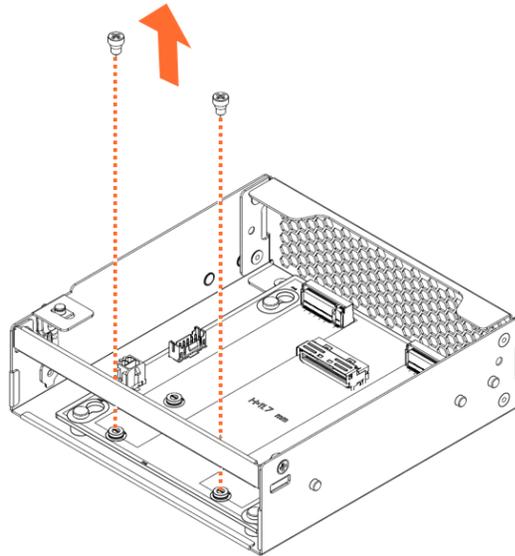


6.11.3 Installing the M.2 SSD

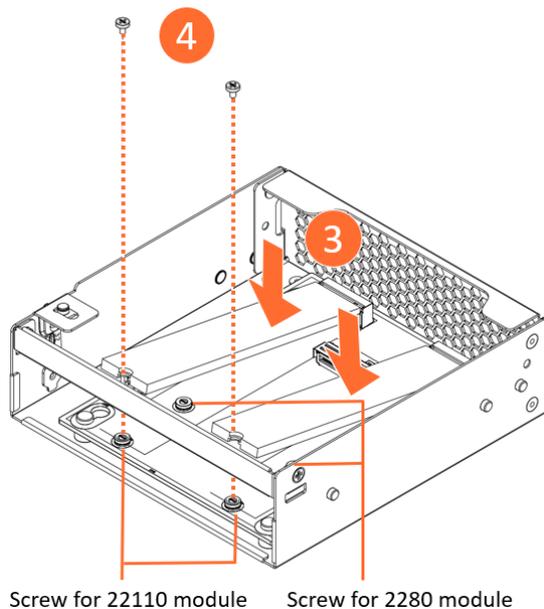
Note:

While the system supports both M.2 22110 and M.2 2280 SSD, the standoffs and screws are pre-installed in the locations for M.2 22110 SSD.

1. [For systems that have no M.2 SSD installed] Remove the M.2 screws pre-installed in the location for M.2 22110 SSD from the M.2 daughter board.



2. [Optional] Remove the M3 standoff from the 22110 location and re-install it to the 2280 location if you want to install an M.2 2280 SSD (torque: 6 ± 0.2 kgf-cm).
3. Install an M.2 SSD to the M.2 daughter board.
4. Install an M.2 screw to secure the M.2 SSD in place (torque: 2 ± 0.2 kgf-cm).
5. Repeat steps 1 to 4 if you want to install another M.2 SSD.



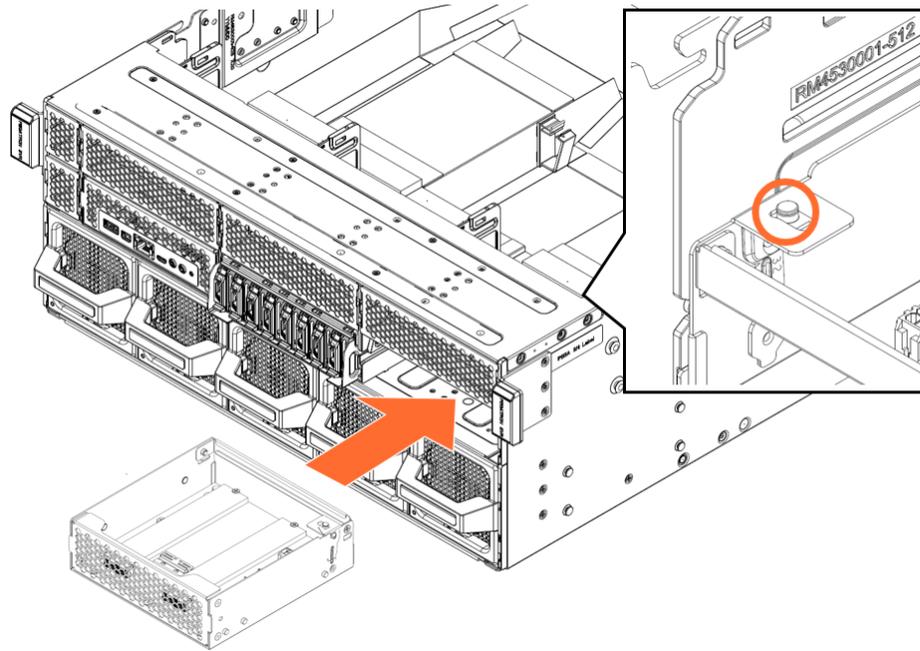
6.11.4 Installing the M.2 SSD Cage

Prerequisites

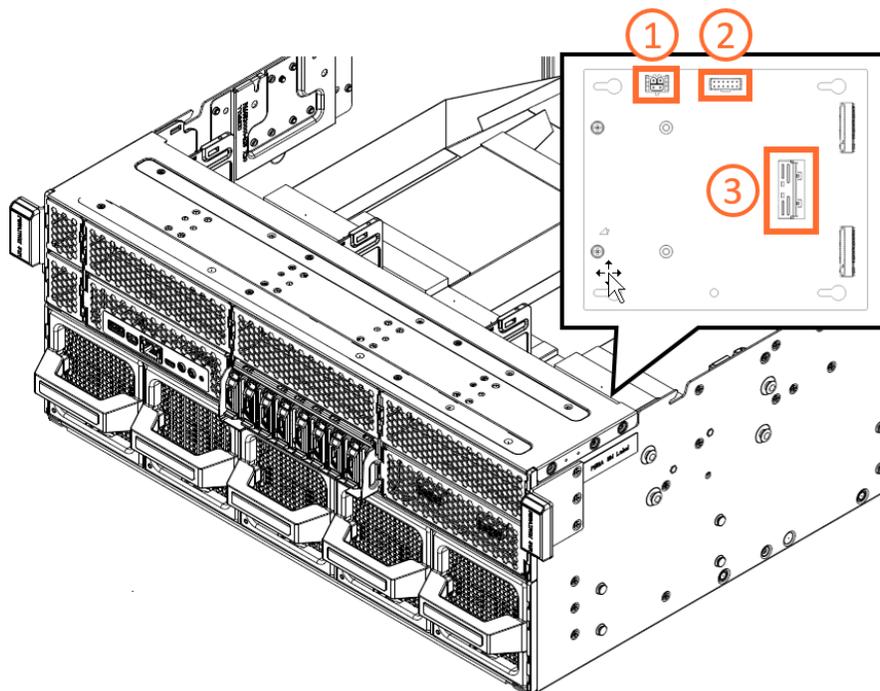
1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, and Top Fan Cage Assembly.

Steps

1. Install the M.2 cage back to the system. Ensure it clicks in place.



2. Connect the (1) M.2/E1.S BP power cable, (2) M.2 sideband cable, and (3) M.2 MCIO cable to the M.2 daughter board.



6.12 Memory Module

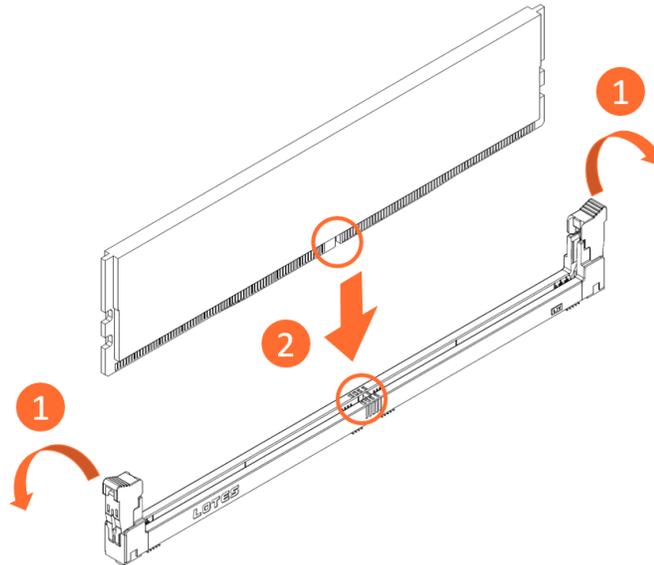
6.12.1 Installing the Memory Module

Prerequisites

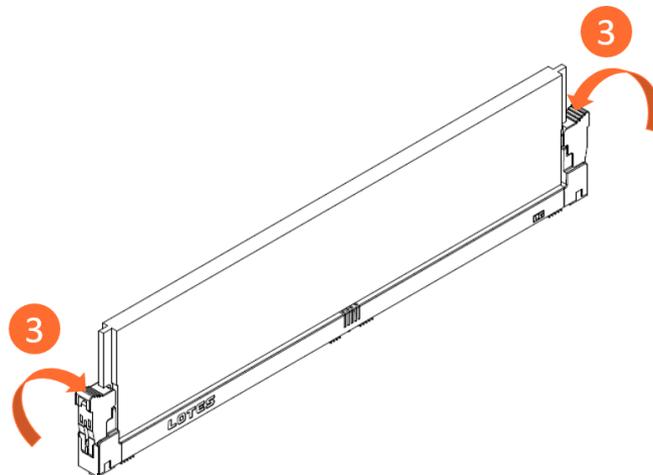
1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, Top Fan Cage Assembly, and Air Duct.

Steps

1. Press the latches outward on both ends of the DIMM slot to unlock it.
2. Align the key of the DIMM module with the respective point on the DIMM slot. Press the DIMM module straight down into the slot and apply pressure evenly on both ends until it locks.



3. Close the side latches and ensure it locks the DIMM module in place.



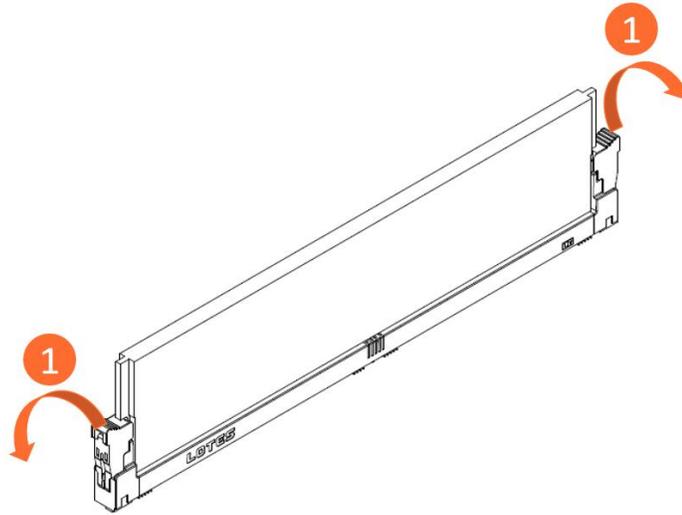
6.12.2 Removing the Memory Module

Prerequisites

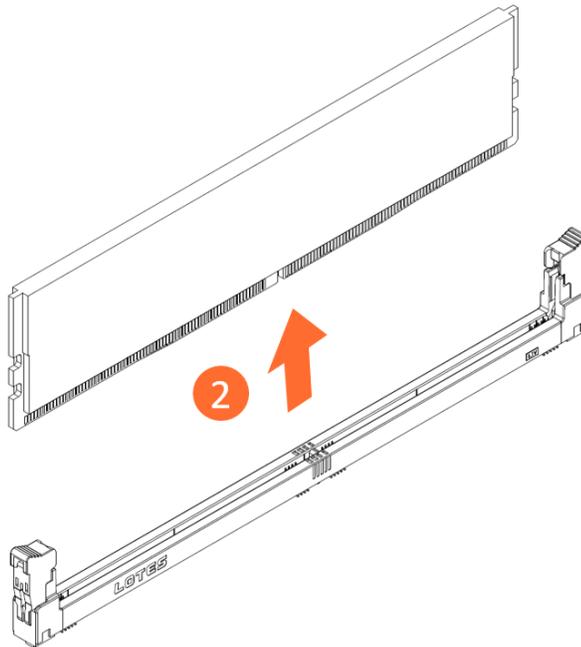
1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, Top Fan Cage Assembly, and Air Duct.

Steps

1. Press the latches outward on both ends of the DIMM slot to unlock it.



2. Lift the DIMM module straight up to remove it from the DIMM slot.



6.13 CPU

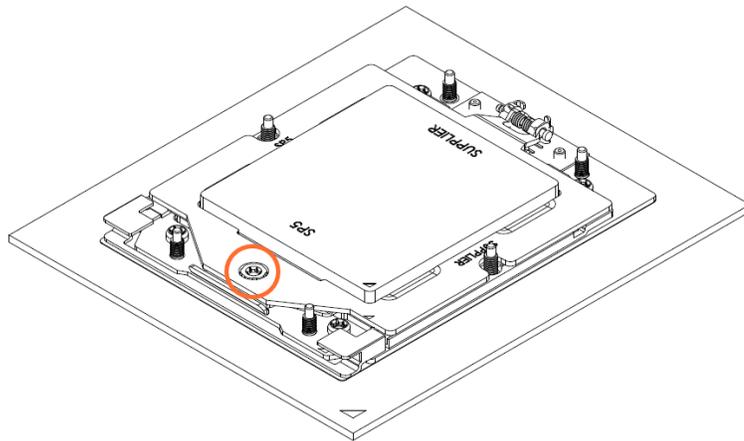
6.13.1 Installing the CPU

Prerequisites

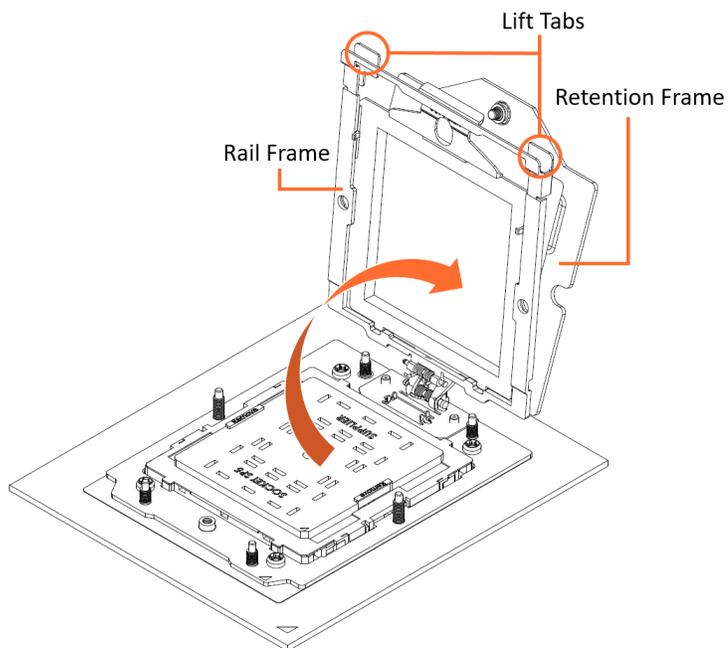
1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, Top Fan Cage Assembly, and Air Duct.

Steps

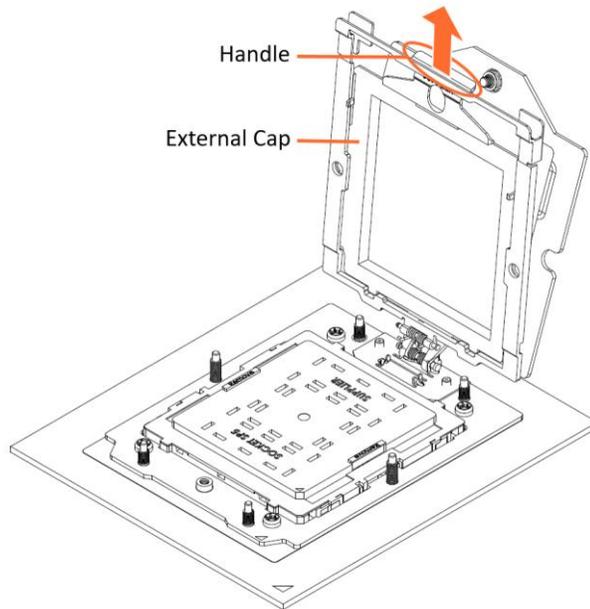
1. Loosen the single captive Torx screw securing the CPU retention frame in place. The spring-loaded frame will then rise up automatically.



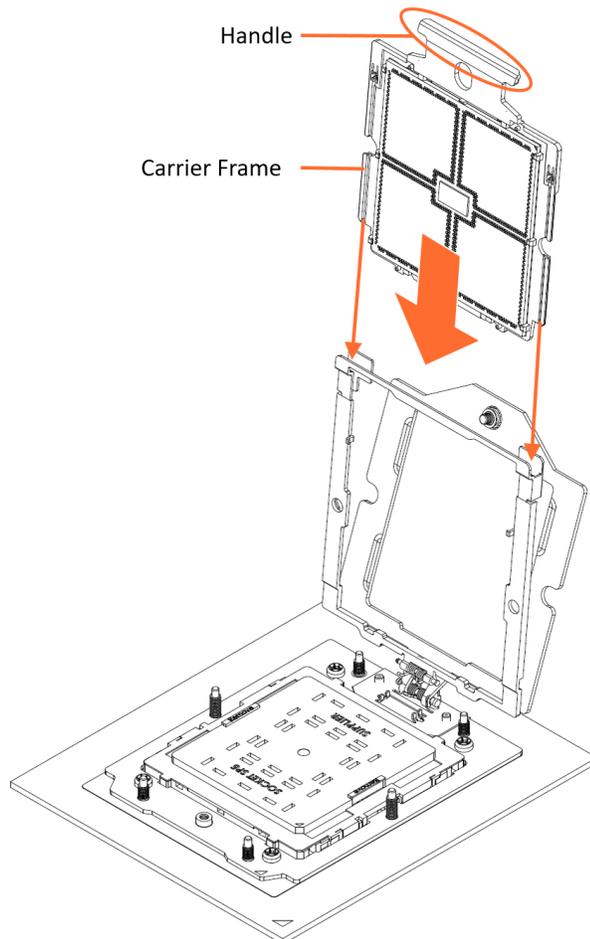
2. Open the retention frame to approximately 105 degrees. Then lift the rail frame by gripping the lift tabs near its front end and open the rail frame to a vertical position.



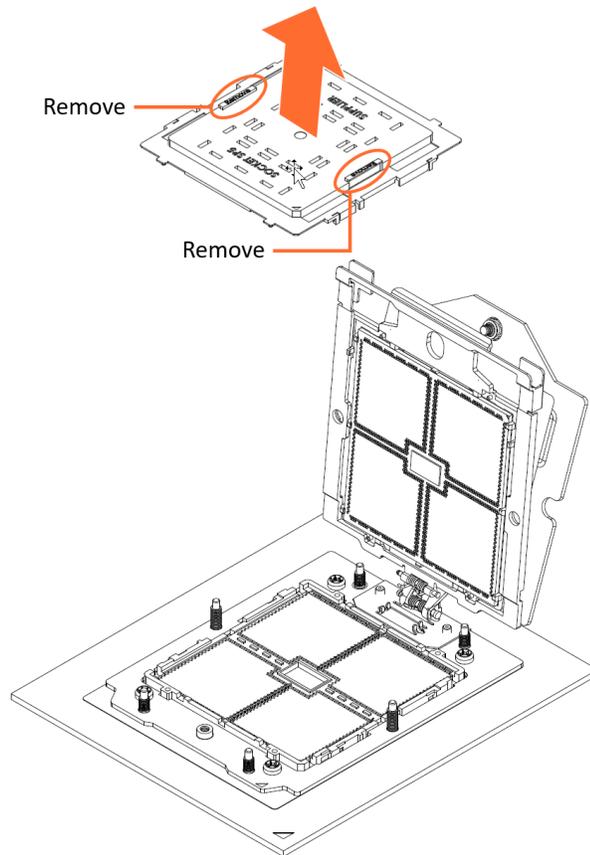
3. Hold the handle of the external cap and lift it upward through the rail guides on the rail frame to remove the cap.



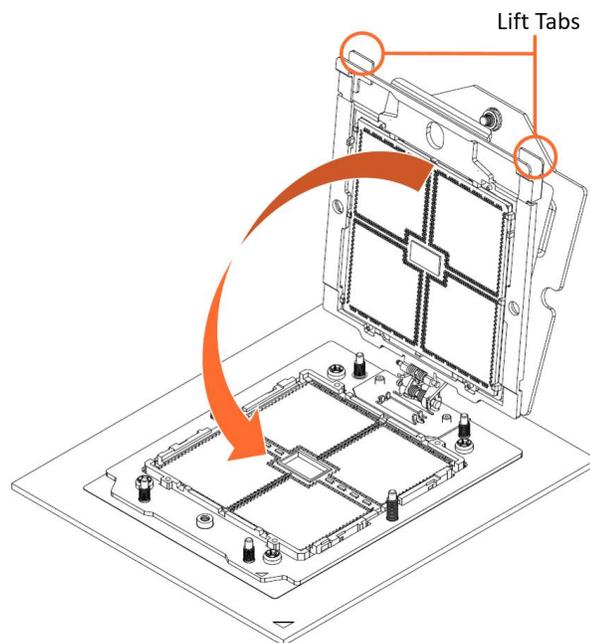
4. CPUs are shipped from the factory with pre-assembled carrier frames. Grip the handle of the carrier frame to lift the CPU package assembly from the CPU package shipping tray. Ensure that the flange features on the carrier frame align with the rail guides on the rail frame and then slide the CPU package assembly downward until it locks with the rail frame.



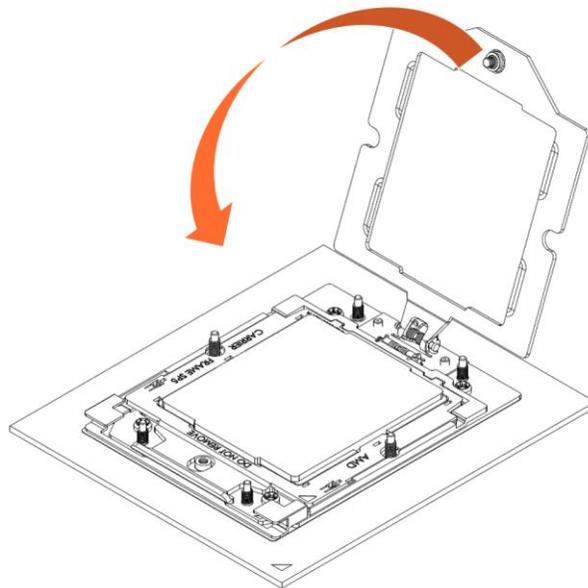
5. Grip the two lift tabs marked **“Remove”** at the middle of the long sides of the cover and lift it up to remove it from the socket housing.



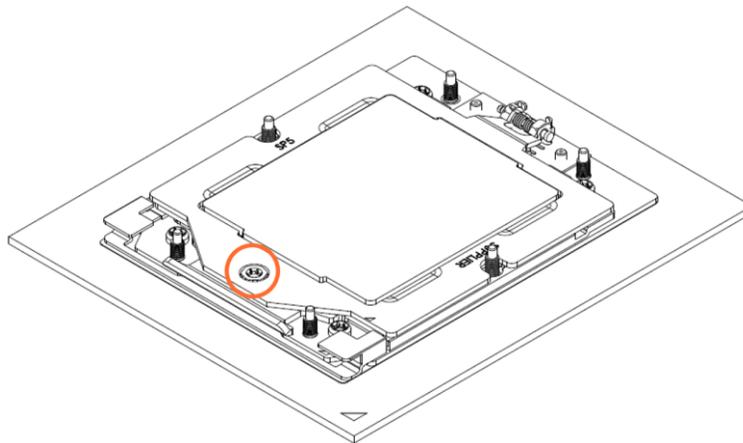
6. Grip the lift tabs at the top of the rail frame and flip the rail frame with the CPU package assembly downward onto the CPU housing until the rail frame engages with the socket housing. Press down the CPU lid to ensure the CPU is properly seated into the socket.



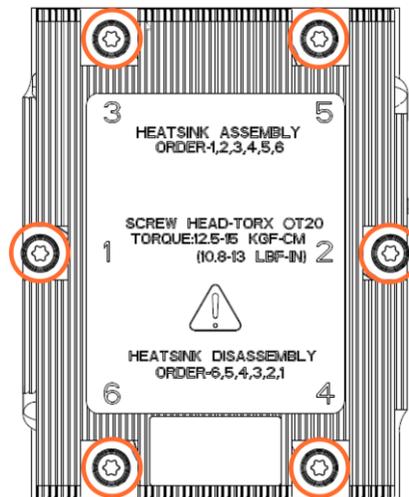
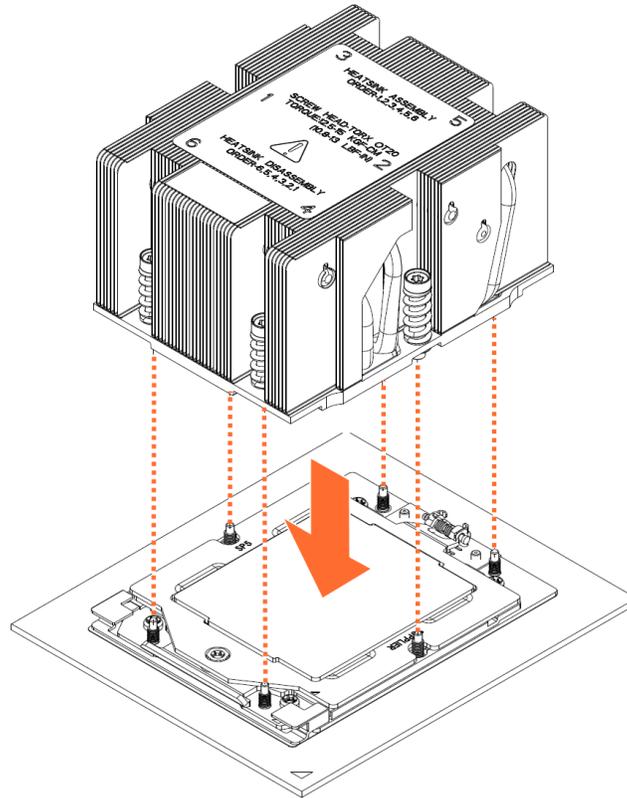
7. Flip the retention frame downward until it is in the horizontal position.



8. Tighten the captive screw to secure the retention frame in place (torque: 13.75 ± 1.25 kgf-cm).



9. Install the heatsink to the CPU and tighten six screws in a diagonal sequence as instructed on the heatsink label (1 > 2 > 3 > 4 > 5 > 6) to secure the heatsink in place (torque: 13.75±1.25 kgf-cm).



Note:

If your server system is not pre-installed with CPU(s) before shipment, after installing CPU(s) by yourself, install the heatsink(s) shipped with the server system, which is pre-applied with thermal grease.

In the situation of CPU replacement where you have to remove an old CPU, install a new CPU, and re-use the heatsink, use alcoholic wipes to clean any residual thermal grease on the heatsink after it is removed from the old CPU, and then apply new thermal grease to the heatsink before it is re-installed to the new CPU.

6.14 CMOS Battery

The CMOS battery is critical for preserving system settings and real-time clock data during power cycles. While the server systems are designed for long-term operation (5+ years), the CMOS battery on the HPM board typically lasts 3-5 years and may require replacement.

Strictly follow the instructions in this user manual when removing the old battery from its holder. Improper removal—such as incorrect steps or tools—can damage the battery holder’s fragile contacts. A compromised holder may lead to poor connectivity, intermittent failures, or even HPM board damage.

Key risks of mishandling include:

- Data loss from corrupted configurations.
- Safety hazards (e.g., battery leakage due to physical stress).

Always power down the server and discharge residual electricity before servicing. Consult Pegatron for technical support if there is any uncertainty. Replace only with compatible batteries and verify holder integrity post-installation. Proactive maintenance ensures server reliability and avoids unnecessary downtime.

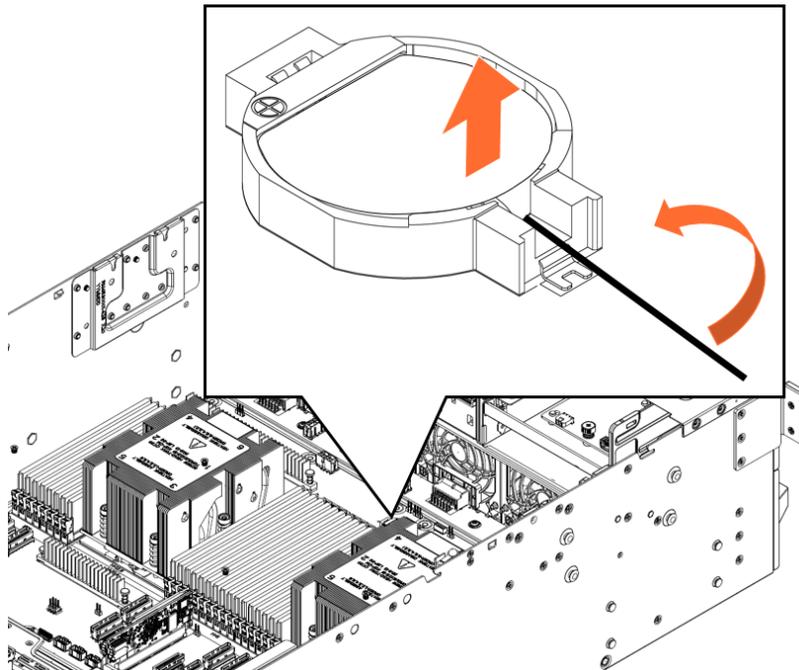
6.14.1 Removing the CMOS Battery

Prerequisites

1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, Top Fan Cage Assembly, and Air Duct.

Steps

1. Use a pin of a diameter smaller than 1.34mm to press the latch on the CMOS battery holder and then pry the battery away from its holder.



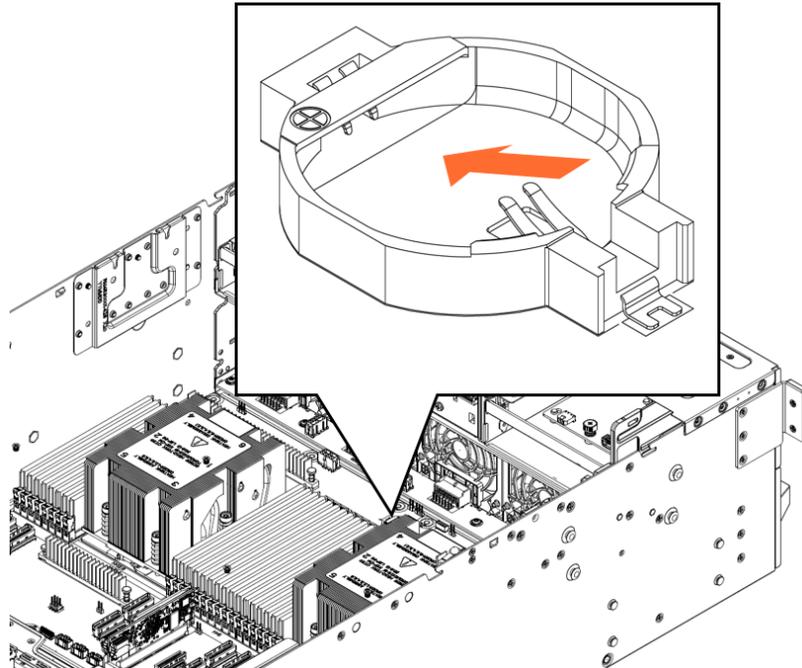
6.14.2 Installing the CMOS Battery

Prerequisites

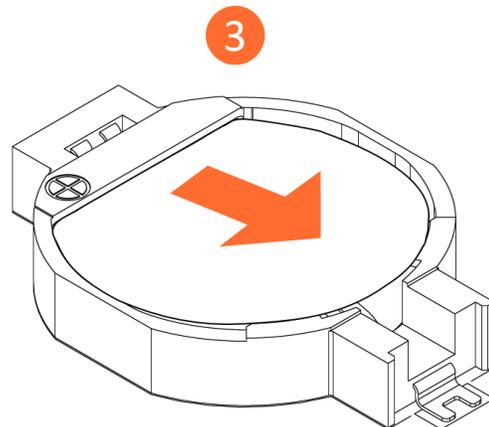
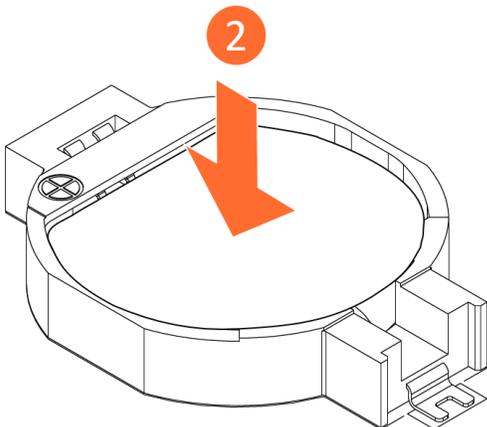
1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, Top Fan Cage Assembly, and Air Duct.

Steps

1. Insert the battery into the battery holder at a tilted angle.



2. Press down the battery until it clicks in place.
3. Slightly push the battery toward the spring of the battery holder to make sure the battery is well seated and secured in place by the spring.



6.15 Switch Board

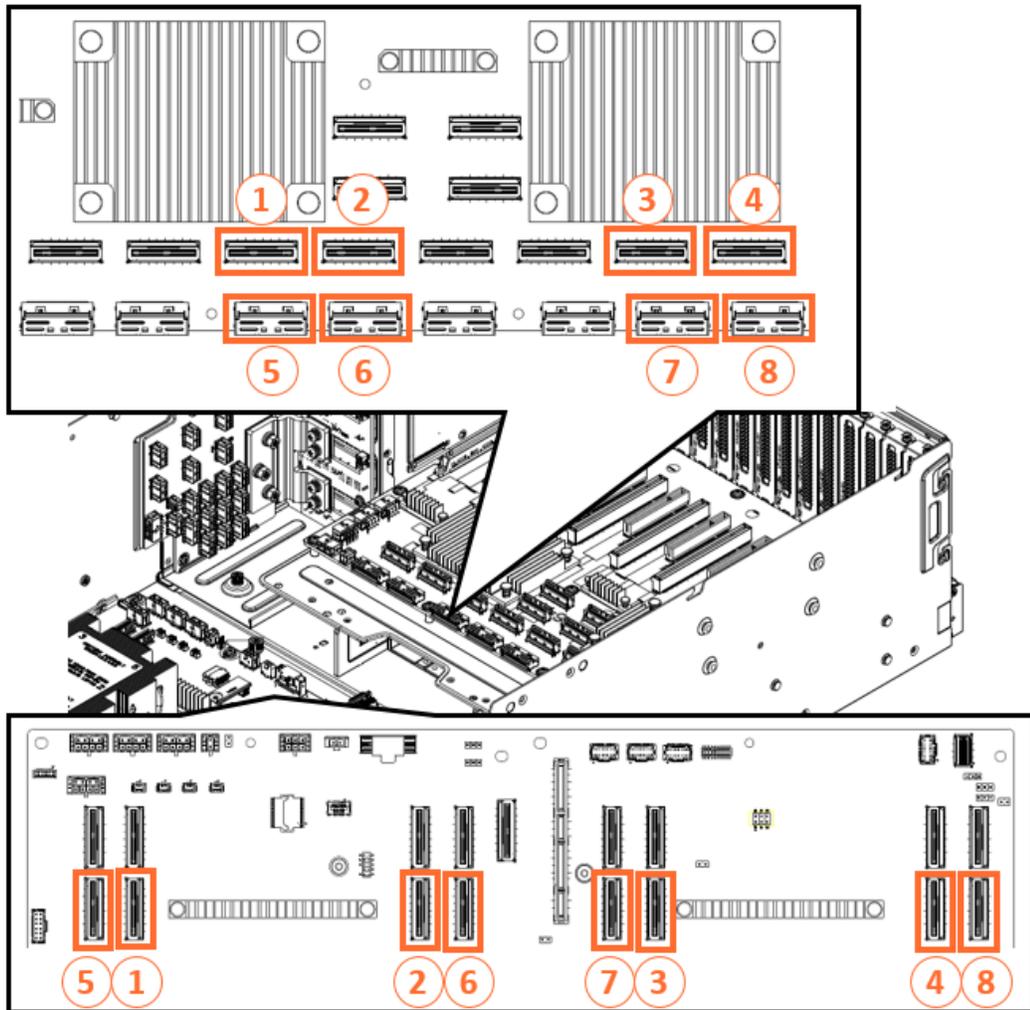
6.15.1 Removing the Switch Board

Prerequisites

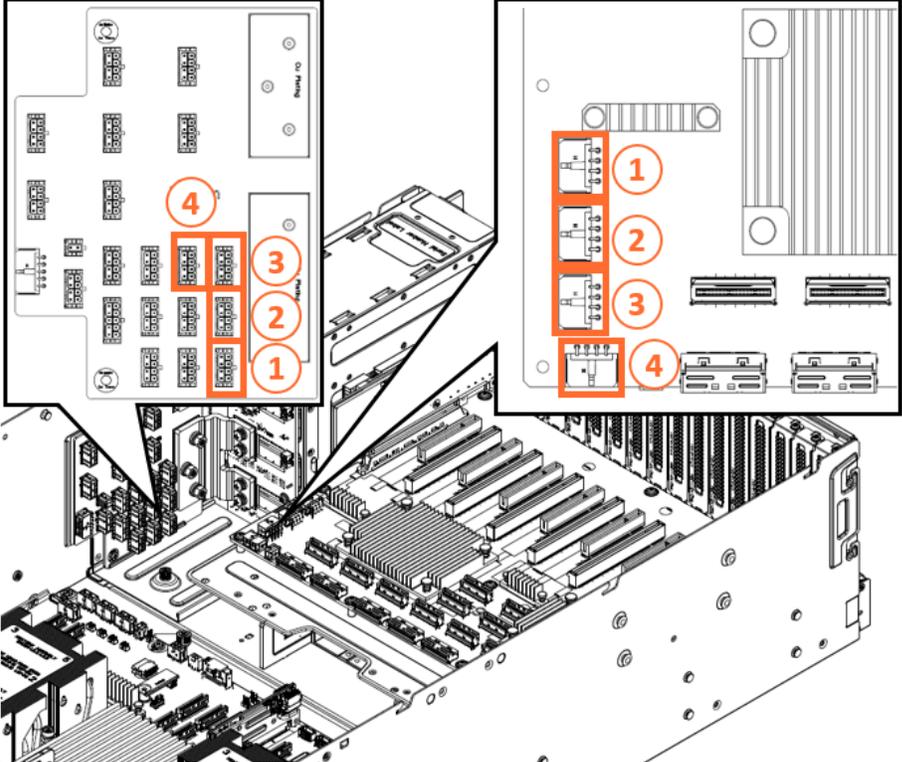
1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, Top Fan Cage Assembly, and Air Duct.

Steps

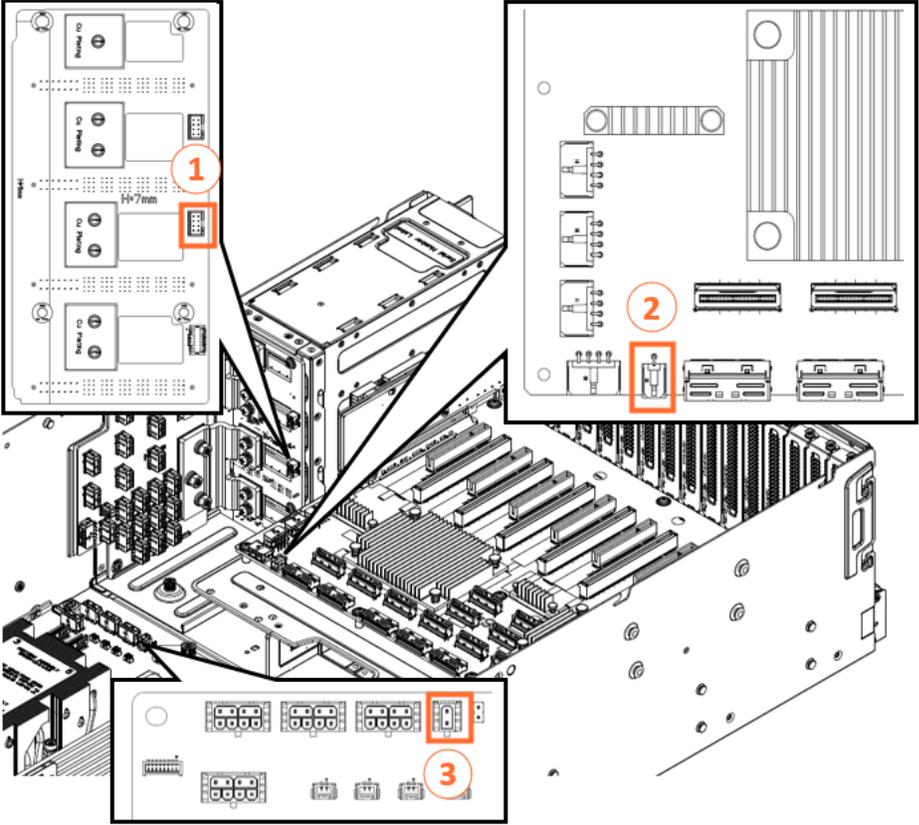
1. Disconnect eight switch MCIO cables from the switch board and HPM board; then remove the eight cables from the system.



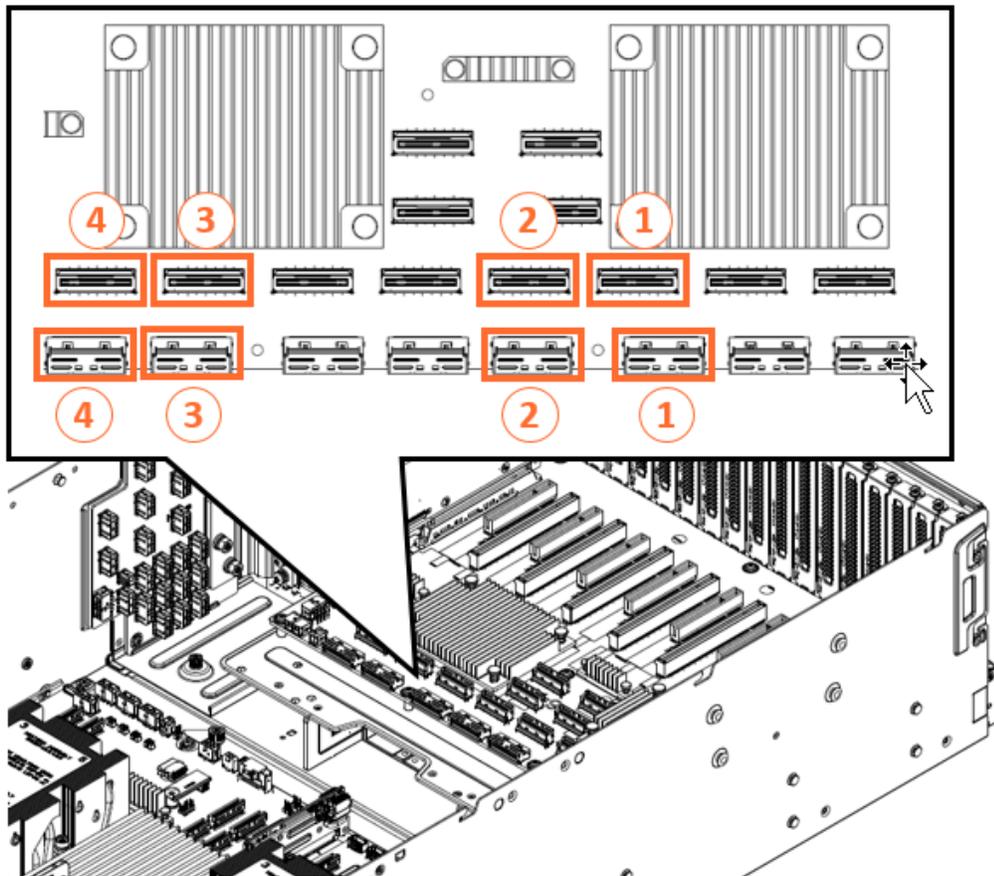
- 2. Disconnect four switch power cables from the switch board and PDB#2; then remove the four power cables from the system.



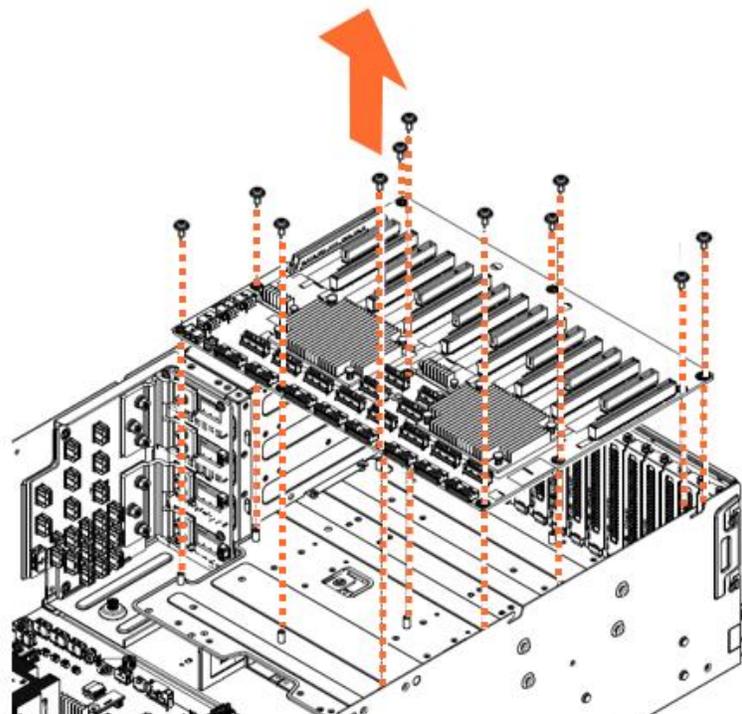
- 3. Disconnect the MB/SW Y-power-cable from the (1) PDB#1, (2) switch board, and (3) HPM board; then remove the Y-cable from the system.



4. [For systems shipped with any add-on card(s)] Disconnect the dual connectors of the following cable(s) from the switch board if applicable: (1) CX7 CEM Riser cable-1, (2) CX7 CEM Riser cable-2, (3) CX7 CEM Riser cable-3, and/or (4) CX7 SW CEM Riser cable.



5. Remove eleven M3 screws securing the switch board in place and then lift up the switch board to remove it from the system.



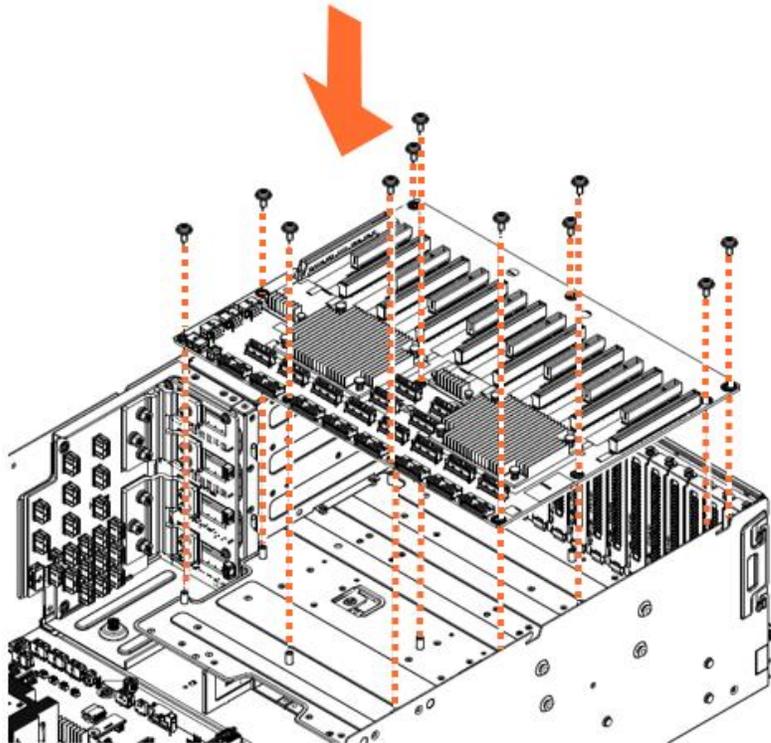
6.15.2 Installing the Switch Board

Prerequisites

1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, Top Fan Cage Assembly, and Air Duct.

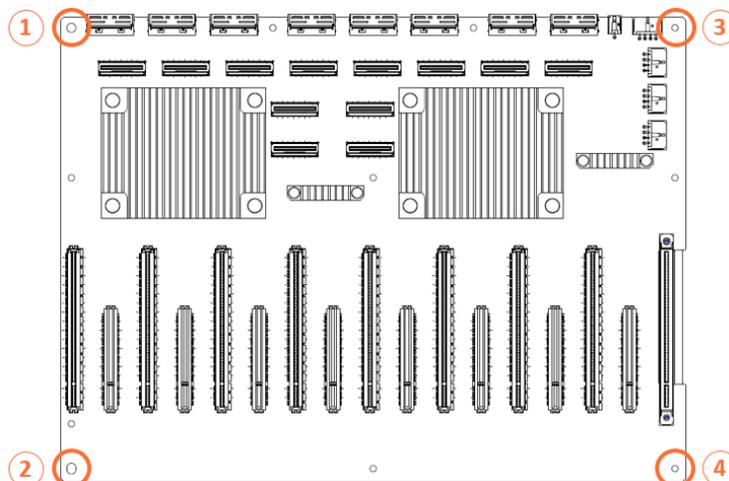
Steps

1. Install the switch board into the system and install eleven M3 screws to secure it in place (torque: 6 ± 0.5 kgf-cm).

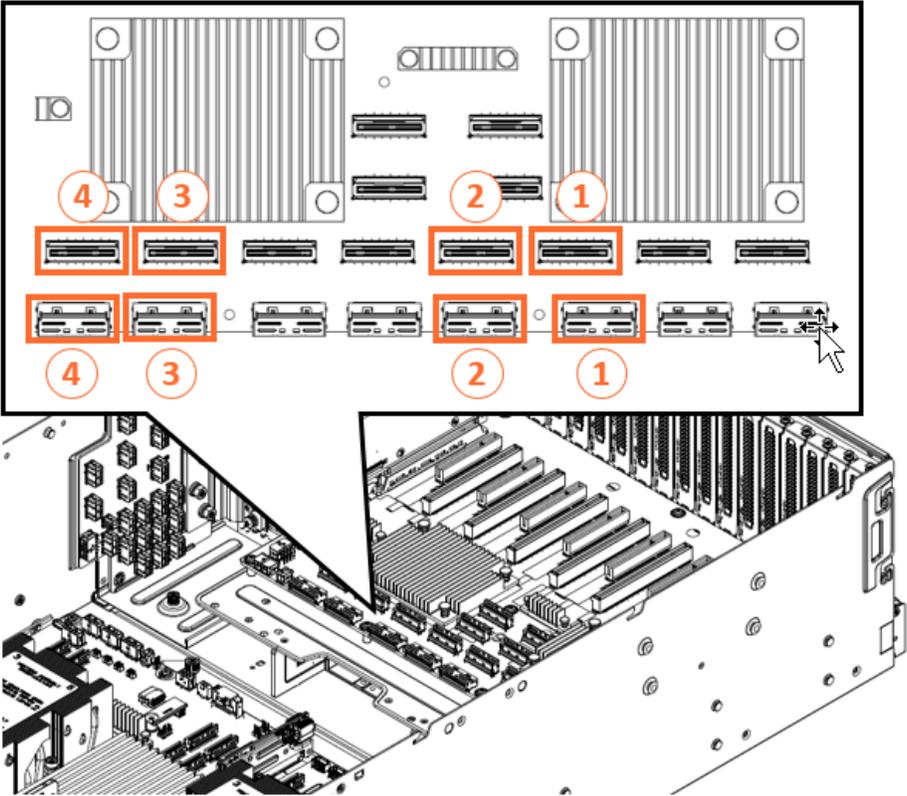


Note:

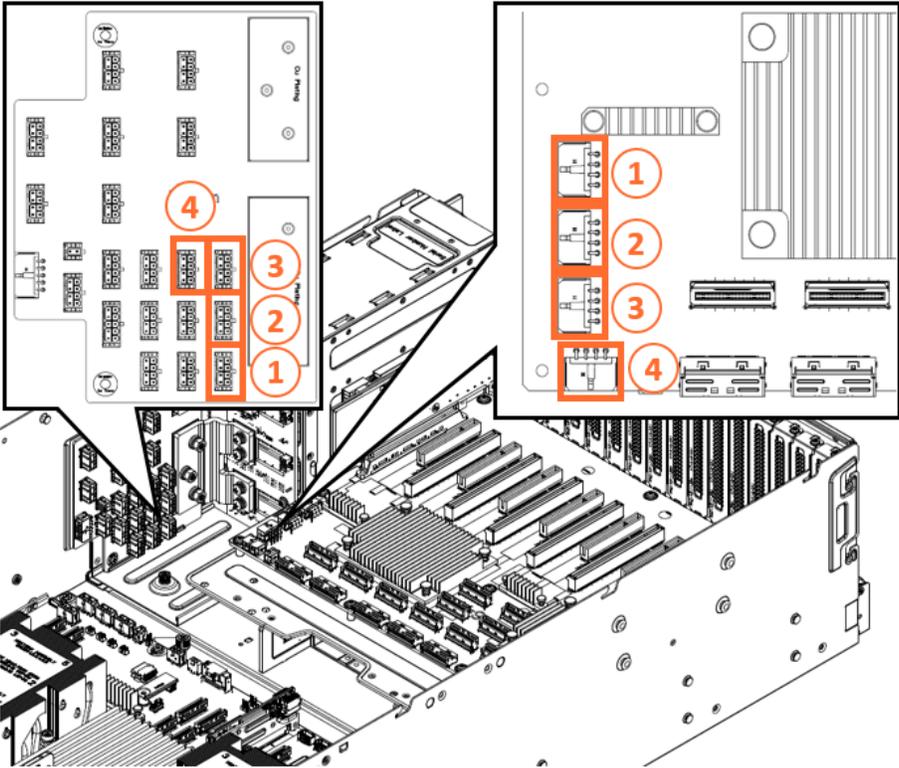
To properly secure the switch board in place, you **MUST** install screws to the four corners of the switch board first in the sequence as indicated below (1 > 2 > 3 > 4) and then install the remaining seven screws.



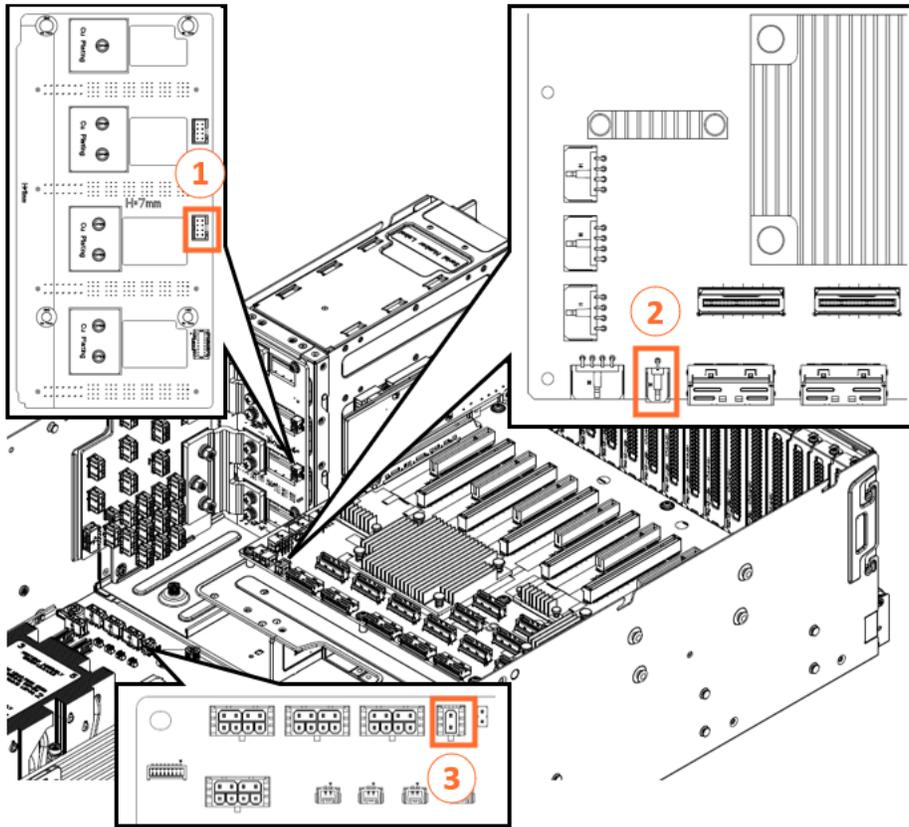
- 2. [For systems shipped with any add-on cards] Connect the dual connectors of the following cable(s) to the switch board if applicable: (1) CX7 CEM Riser cable-1, (2) CX7 CEM Riser cable-2, (3) CX7 CEM Riser cable-3, and/or (4) CX7 SW CEM Riser cable.



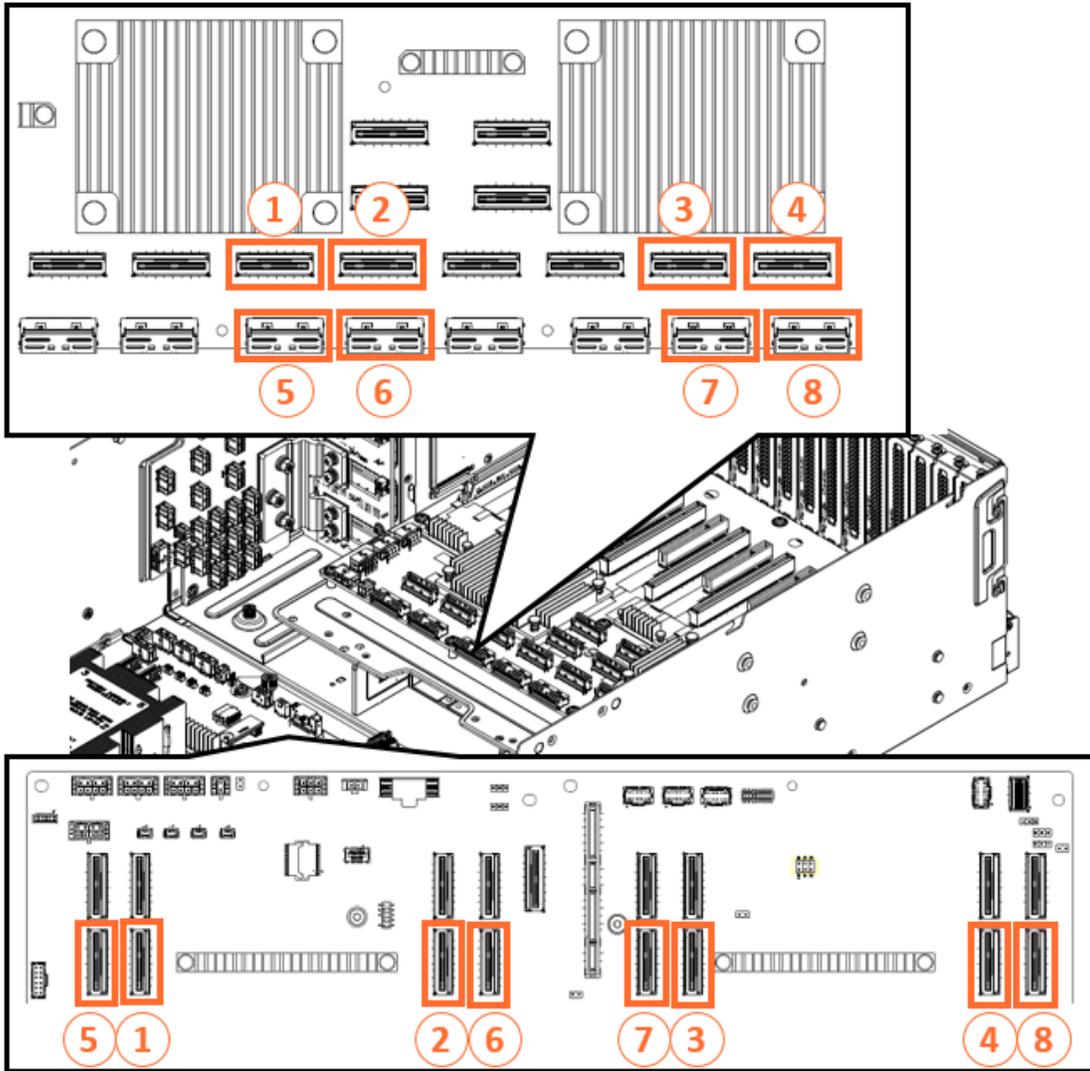
- 3. Connect the four switch power cables to the switch board and PDB#2.



4. Connect the MB/SW Y-power-cable to the (1) PDB#1, (2) switch board, and (3) HPM board.



5. Connect the eight switch MCIO cables to the switch board and HPM board.



6.16 Right FHFL Add-On Card (Add-On_4)

Note:

If necessary, remove the GPU card(s) adjacent to the Add-on_4 slot to make more space for the removal or installation of the right add-on card.

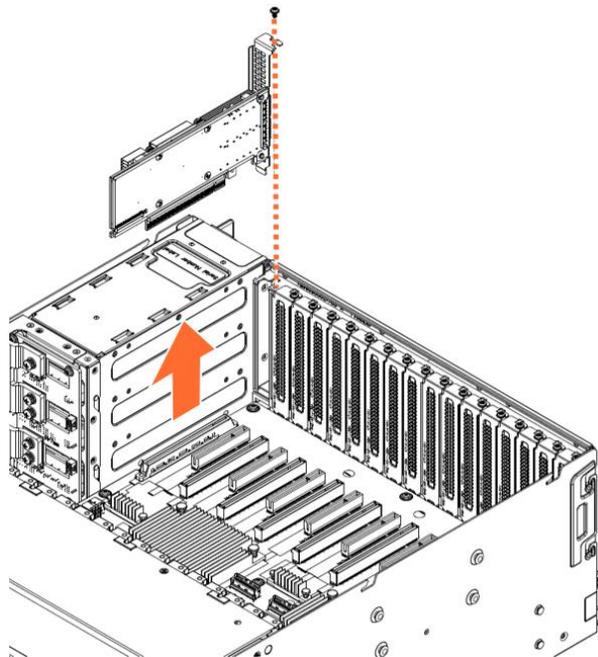
6.16.1 Removing the Add-On_4 Card

Prerequisites

1. AC power off the system.
2. Remove Top Cover.

Steps

1. Remove single M3 screw securing the add-on_4 card in place and then remove the card.



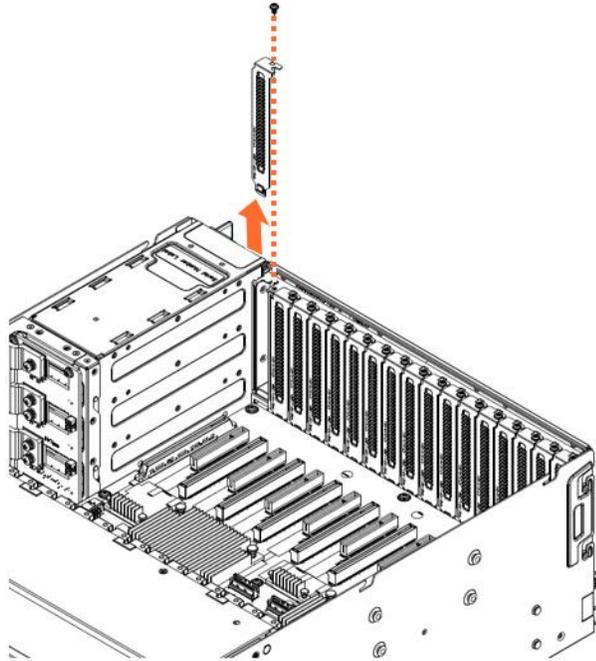
6.16.2 Installing the Add-On_4 Card

Prerequisites

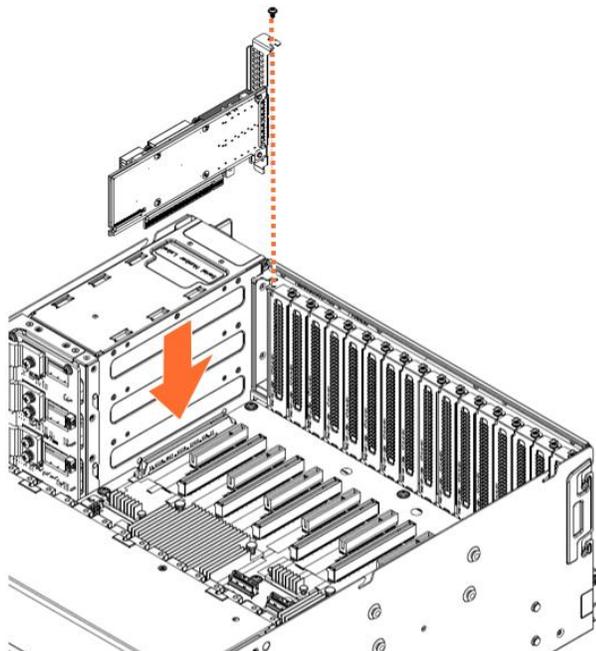
1. AC power off the system.
2. Remove Top Cove.

Steps

1. [For systems shipped without a PCIe card installed in the Add-on_4 slot] Remove the single M3 screw securing the dummy PCIe bracket in place and then remove the bracket.



2. Insert the add-on card to the add-on_4 slot on the switch board and then install the single M3 screw to secure the add-on card in place (torque: 6 ± 0.5 kgf-cm).



6.17 HHL Add-On Card (Add-On_3)

Note:

As the add-on_3 slot is located under the PCIe Switch board and at the same PCIe tray as the rear IO daughter board, you must remove and install the rear IO daughter board together with the add-on_3 card.

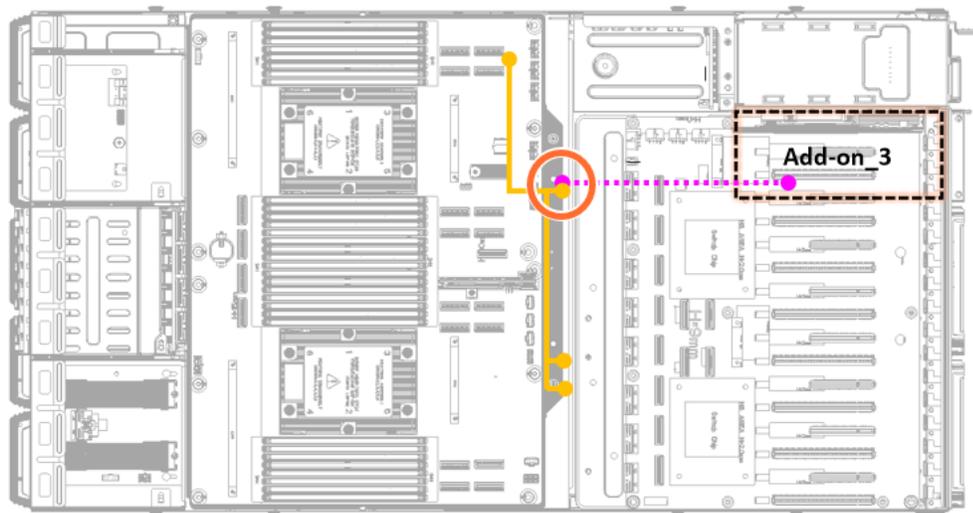
6.17.1 Removing the Add-on_3 Card

Prerequisites

1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, Top Fan Cage Assembly, and Air Duct.

Steps

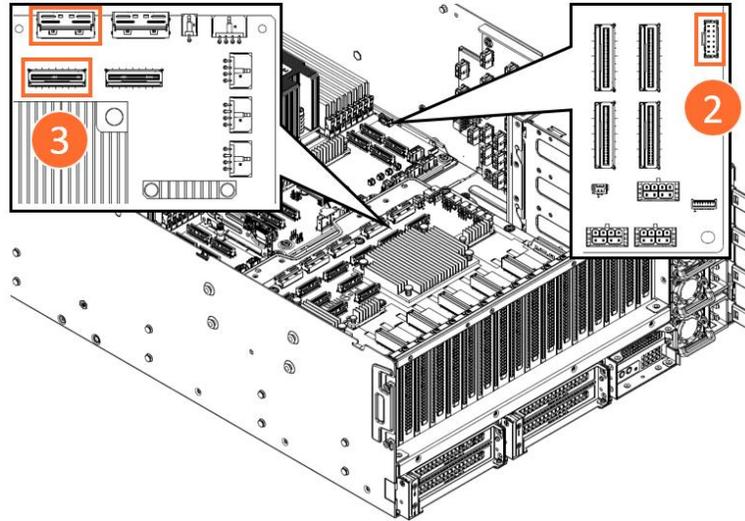
1. Disconnect the power connector of the riser cable from the riser power switch cable.



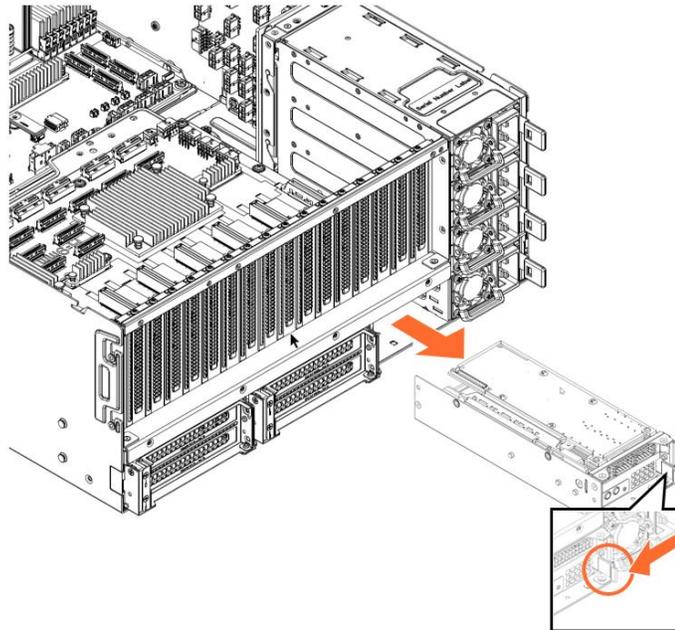
Note:

The Add-on_3 card is installed under the switch board tray and the riser cable is routed under the switch board tray.

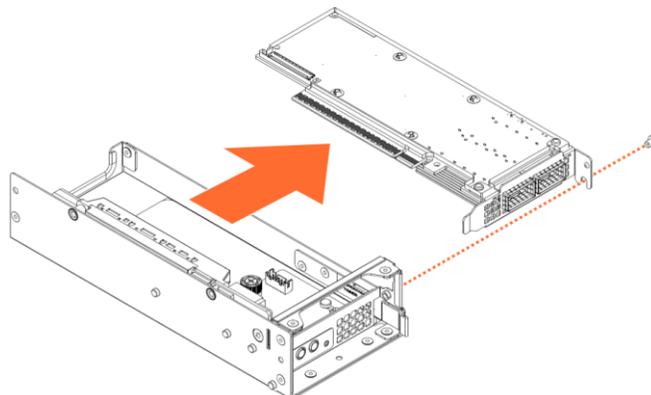
2. Disconnect the rear IO sideband cable from the HPM board.
3. Disconnect the two MCIO connectors of the add-on_3 CEM riser cable from the switch board.



4. Sliding the PCIe tray out of the system while pushing the latch on the PCIe tray to its left side.



5. Remove the single #6-32 screw securing the add-on card to the tray and then separate the card from the tray.



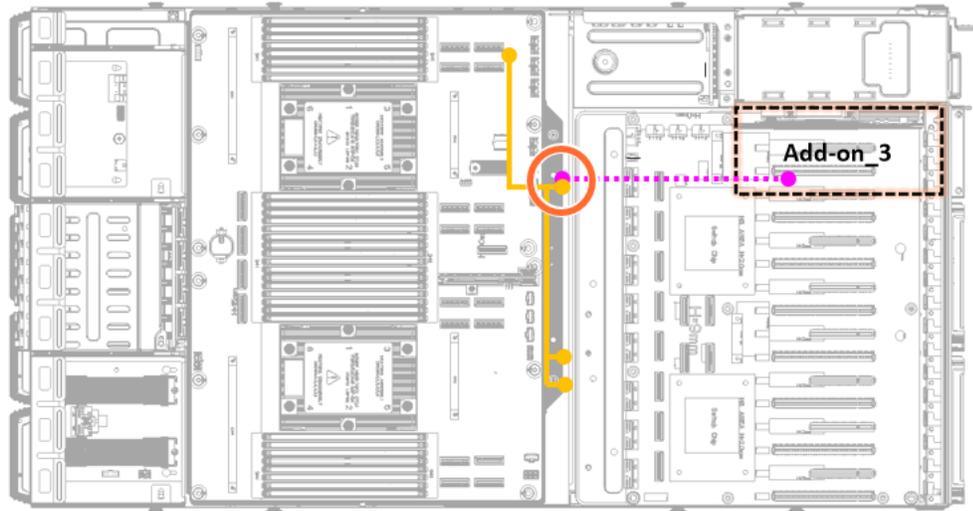
6.17.2 Installing the Add-on_3 Card (Add-on_3)

Prerequisites

1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, Top Fan Cage Assembly, and Air Duct.

Steps

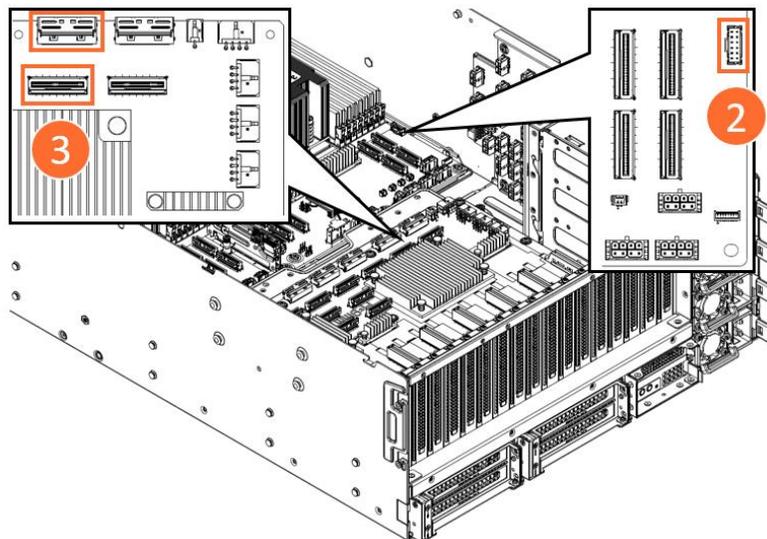
1. Disconnect the power connector of the riser cable from the riser power switch cable.



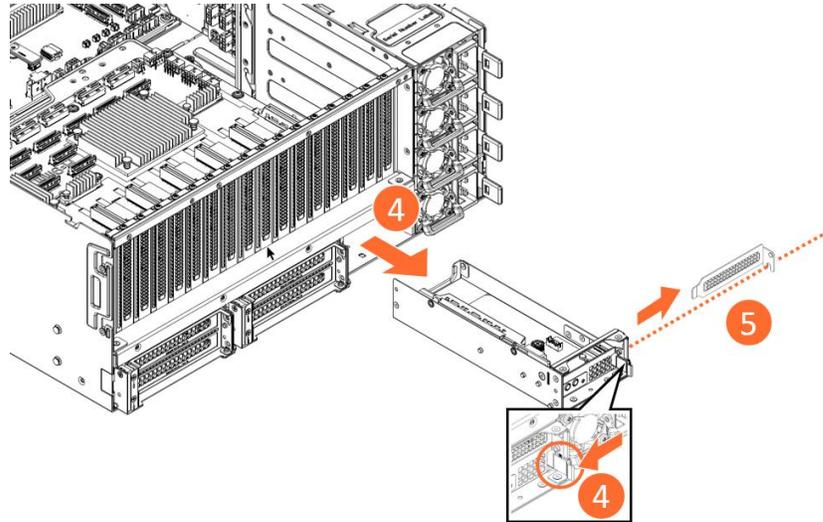
Note:

The Add-on_3 card is to be installed under the switch board tray and the riser cable is routed under the switch board tray.

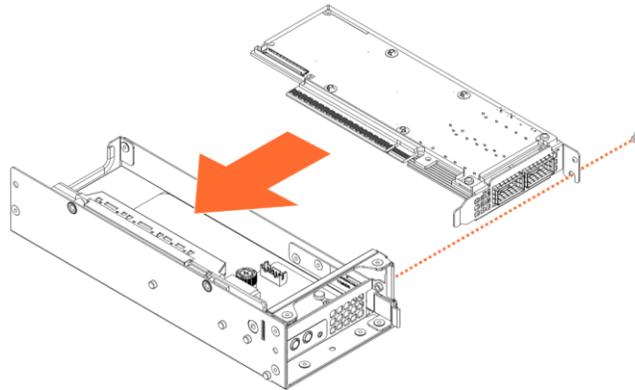
2. Disconnect the rear IO sideband cable from the HPM board.
3. Disconnect the two MCIO connectors of the add-on_3 CEM rise cable from the switch board.



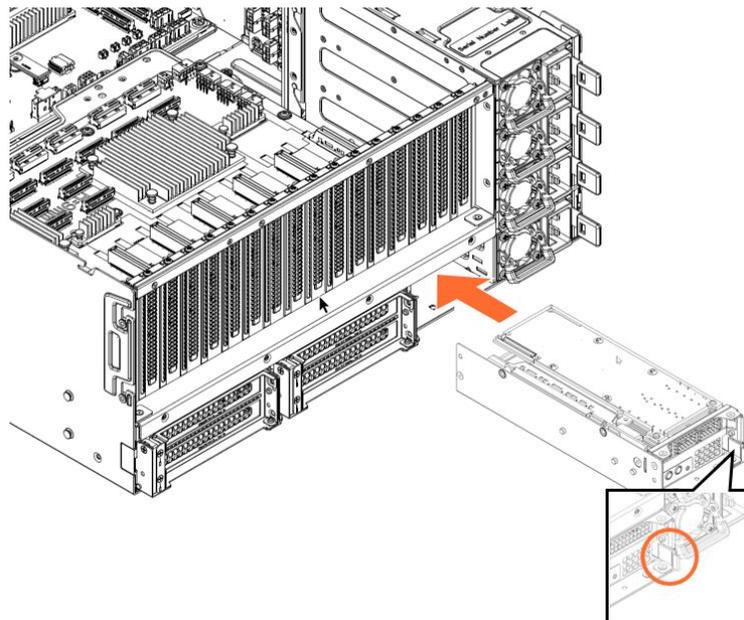
4. Sliding the PCIe tray out of the system while pushing the latch on the PCIe tray to its left side.
5. [For systems shipped without an add-on card installed in the Add-on_3 slot] Remove the single #6-32 screw securing the PCIe dummy bracket to the tray and then remove the bracket from the tray.



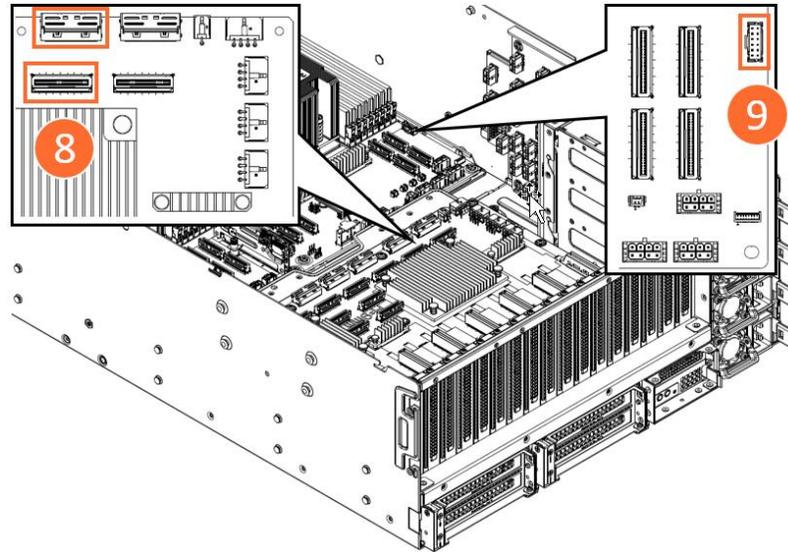
6. Insert the add-on card to the rider cable-3 connector on the tray and then install the single #6-32 screw to secure the add-on card to the tray (torque: 9 ± 0.5 kgf-cm).



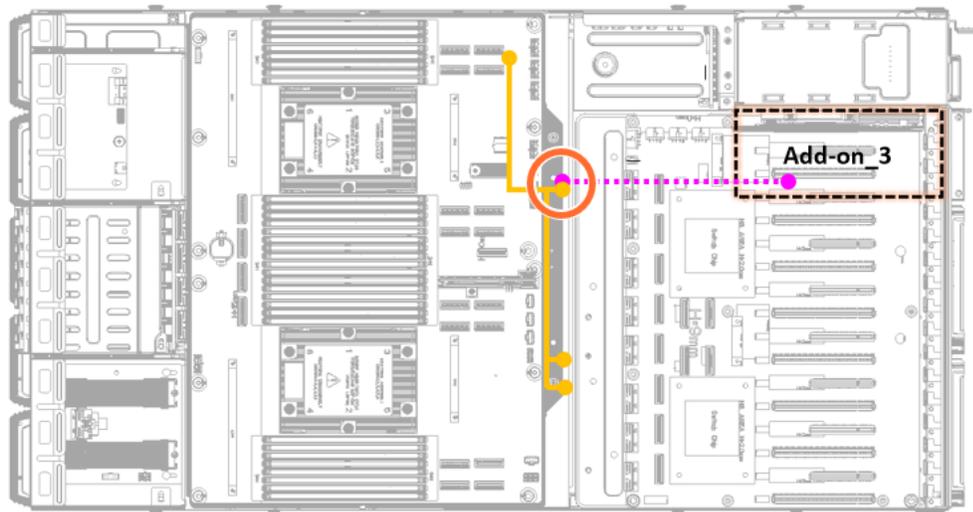
7. Install the add-on card assembly to the server. Ensure the latch is locked in place.



8. Connect the two MCIO connectors of the add-on_3 CEM rise cable-3 to the switch board.
9. Connect the rear IO sideband cable to the HPM board.



10. Connect the power connector of the riser cable to the riser power switch cable.



Note:

The riser cable is routed under the switch board tray.

6.18 Left FHFL Add-On Cards (Add-On_0 and Add-On_1)

Note:

As the Add-on_0 and Add-on_1 slots both locate under the PCIe Switch board and on the left PCIe tray (As you face to the system rear side) and the two cards must be removed and installed together with the PCIe tray as an assembly, in the instructions below both slots are installed with a card. You can skip some of the steps if your system only has one add-on card installed to the left PCIe tray(As you face to the system rear side).

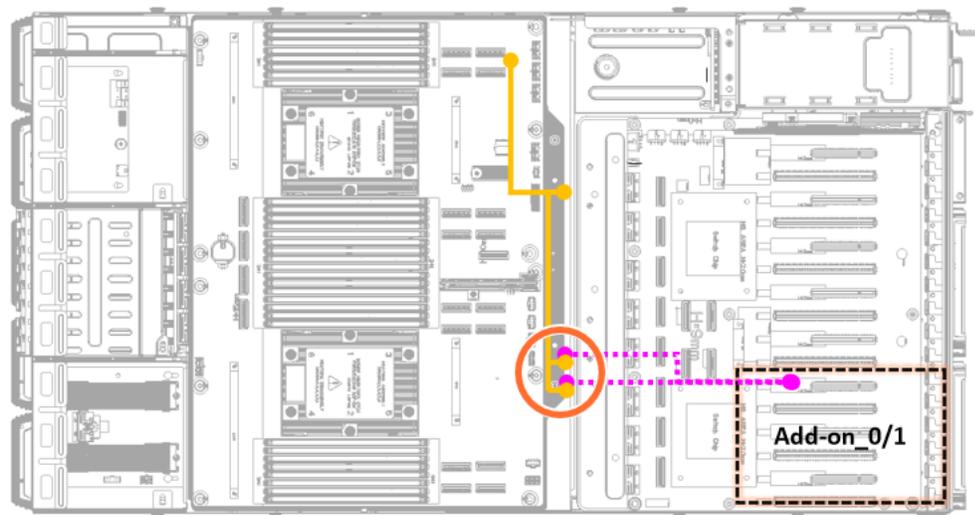
6.18.1 Removing the Add-on_0 and Add-on_1 Card

Prerequisites

1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, Top Fan Cage Assembly, Air Duct, and Switch Daughter Board.

Steps

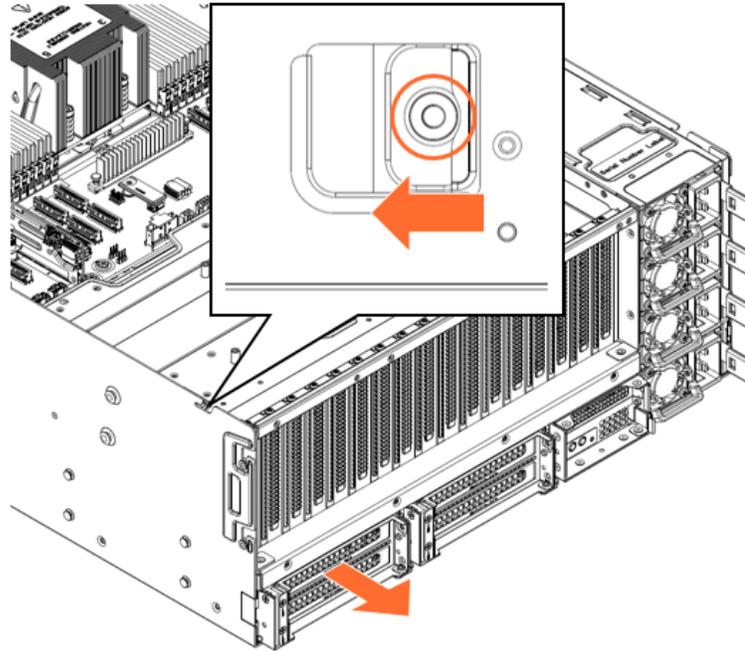
1. Disconnect the power connectors of the riser cable from the riser power switch cable.



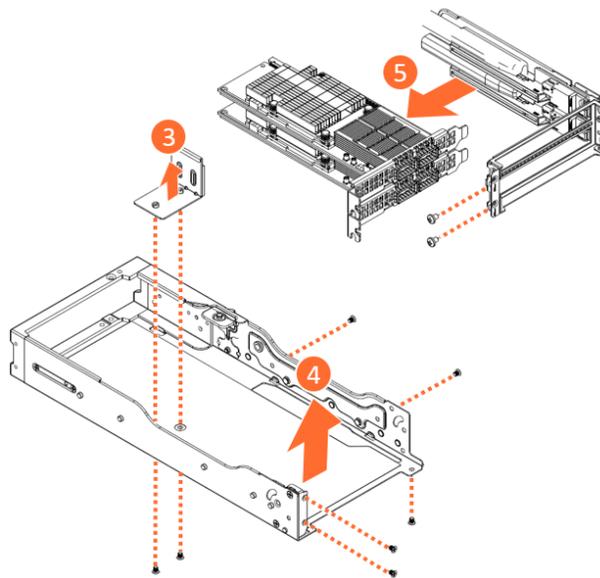
Note:

The Add-on_0 and Add-on_1 cards are installed under the switch board tray and the riser cable is routed under the switch board tray.

2. Use one hand to apply force with a tool (e.g. a scribe) to the latch on the switch board tray (the one above the left PCIe tray) while using the other hand to pull the PCIe tray out of the system.



3. Remove two M3 screws securing the stopper bracket to the PCIe tray and then remove the stopper bracket.
4. Remove five M3 screws securing the L-bracket to the PCIe tray and then remove the L-bracket with the add-on_0 card and add-on_1 card.
5. Remove the two M3 screws securing the add-on cards to the L-bracket and then separate the cards from the bracket.



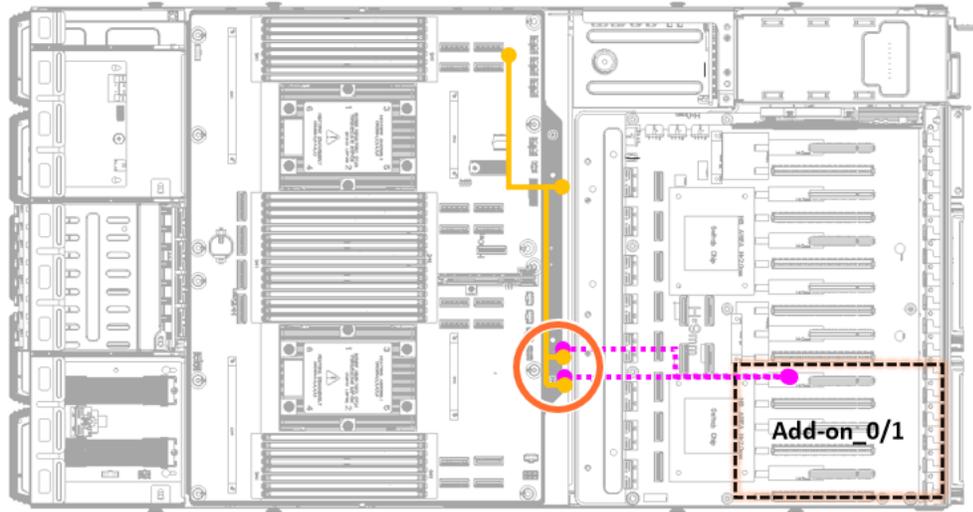
6.18.2 Installing the Add-on_0 and Add-on_1 Card

Prerequisites

1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, Top Fan Cage Assembly, Air Duct, and Switch Daughter Board.

Steps

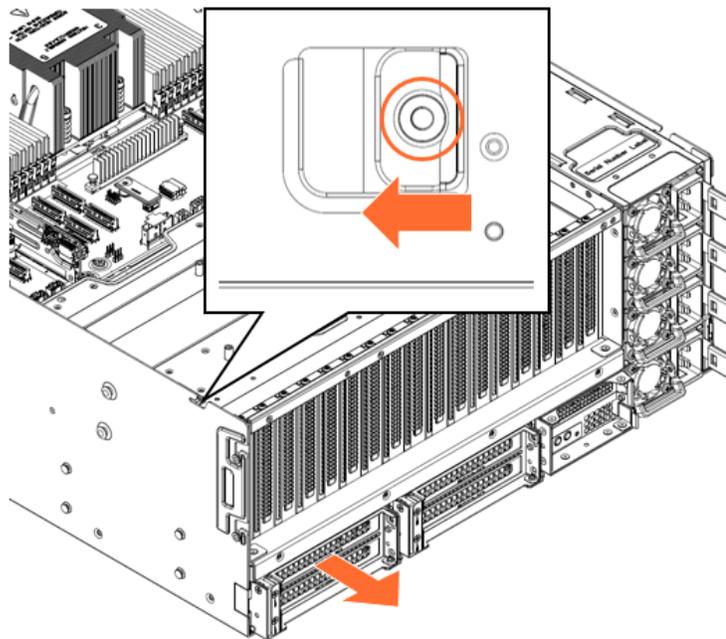
1. Disconnect the power connector of the riser cable from the riser power switch cable.



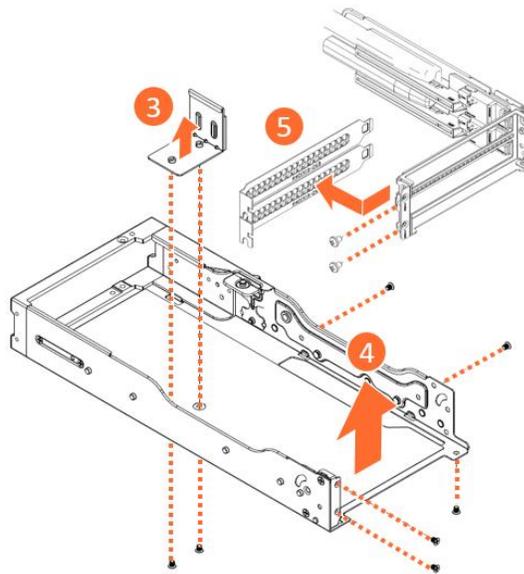
Note:

The Add-on_0 and Add-on_1 cards are to be installed under the switch board tray and the riser cable is routed under the switch board tray.

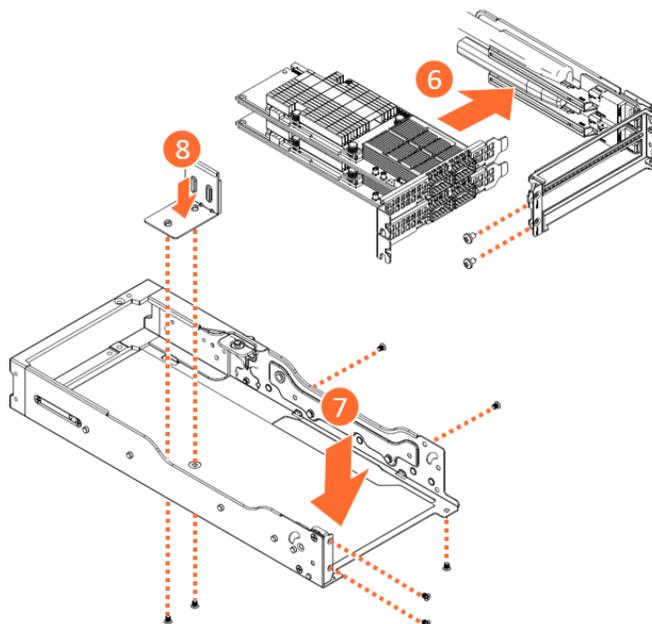
2. Use one hand to apply force with a tool (e.g. a scribe) to the latch on the switch board tray (the one above the left PCIe tray) while using the other hand to pull the PCIe tray out of the system.



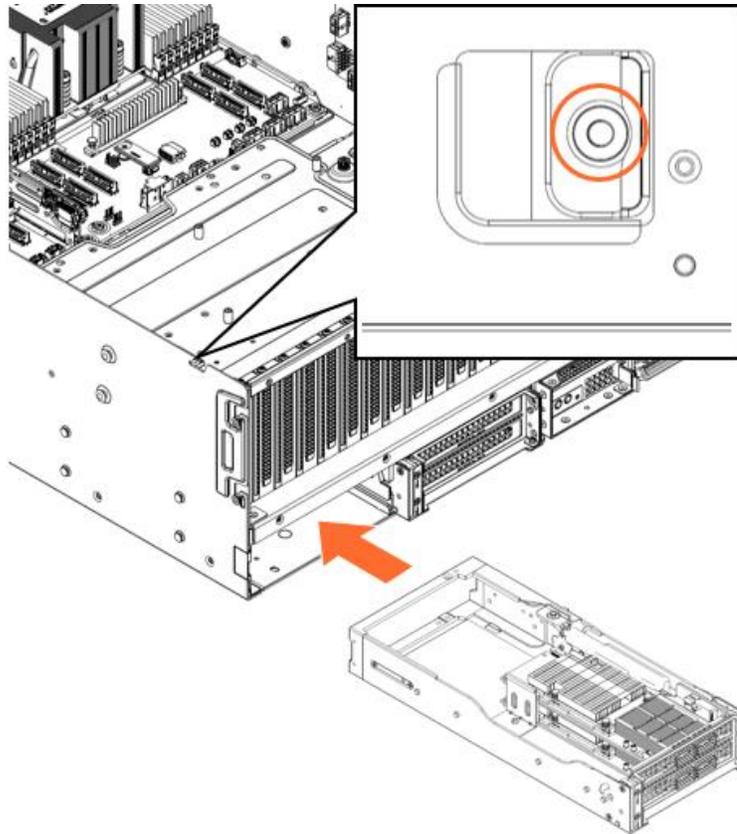
3. Remove two M3 screws securing the stopper bracket to the PCIe tray and then remove the stopper bracket.
4. Remove five M3 screws securing the L-bracket to the PCIe tray and then remove the L-bracket from the tray.
5. [For systems shipped without add-on cards installed in the Add-on_0 and Add-on_1 slots] Remove two M3 screws securing the PCIe dummy brackets to the tray and then remove the brackets from the tray.



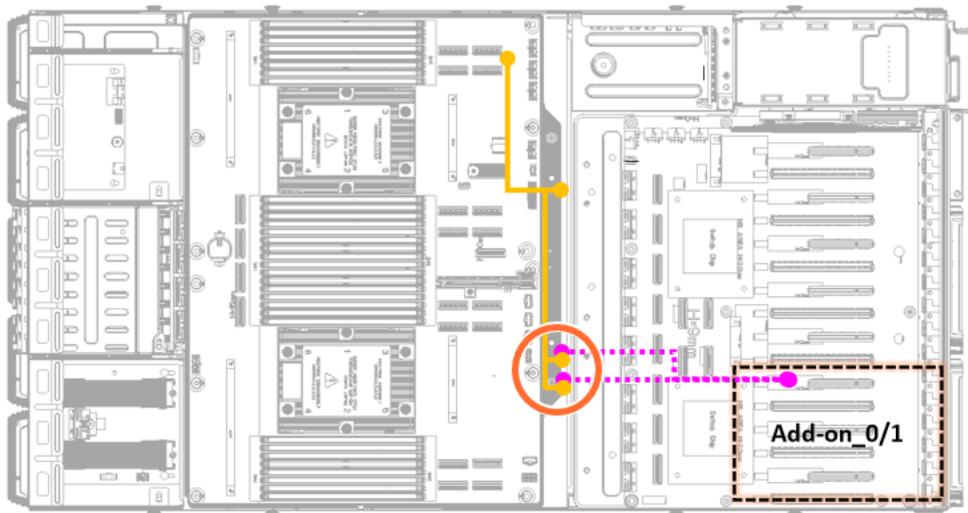
6. Insert the add-on_0 card and add-on_1 card into the riser cable connectors on the L-bracket and then install two M3 screws to secure the add-on cards to the L-bracket (torque: 6 ± 0.5 kgf-cm).
7. Install the L-bracket with add-on cards to the PCIe tray while threading the riser cable through the rear opening of the tray. Then install five M3 screws to secure the L-bracket to the PCIe tray (torque: 6 ± 0.5 kgf-cm).
8. Install the stopper bracket to the tray, ensure it secures the add-on cards in place, and then install two M3 screws to secure the stopper bracket in place (torque: 6 ± 0.5 kgf-cm).



9. Install the PCIe tray with add-on cards assembly back to the system. Ensure the latch is locked in place.



10. Connect the power connector of the riser cable to the riser power switch cable.



Note:

The riser cable is routed under the switch board tray.

6.19 Middle FHFL Add-On Card (Add-On_2)

Note:

As the add-on 2 slot is reserved for a BF3 DPU card by factory default, “BF card” is used in the instructions below as an example.

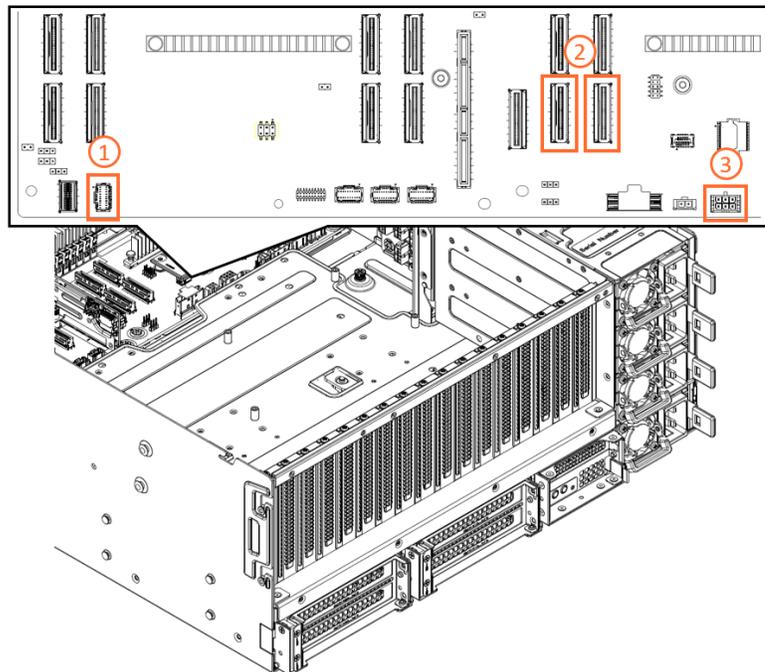
6.19.1 Removing the Add-On_2 Card

Prerequisites

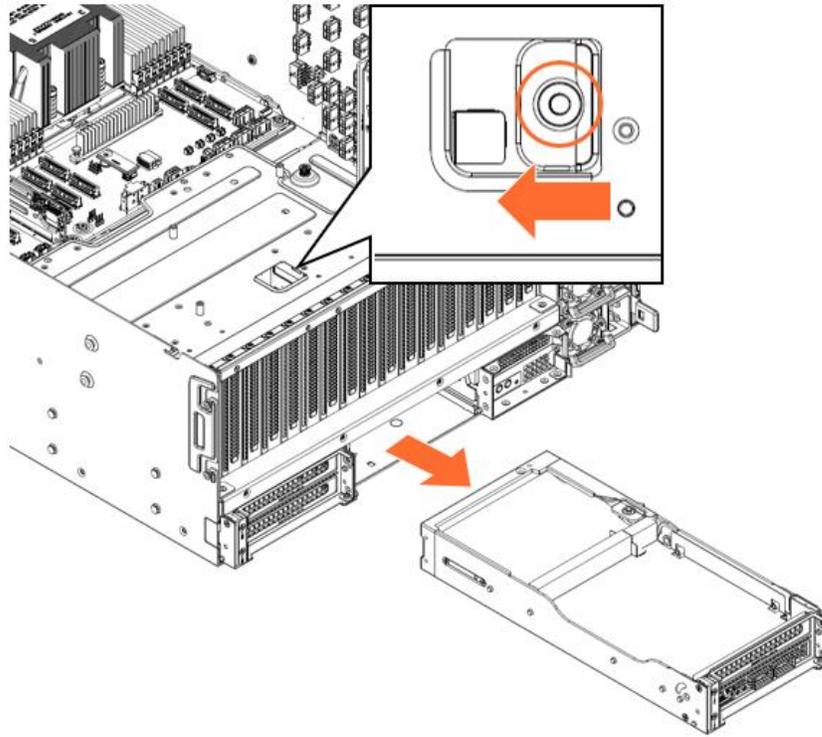
1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, Top Fan Cage Assembly, Air Duct, and Switch Daughter Board.

Steps

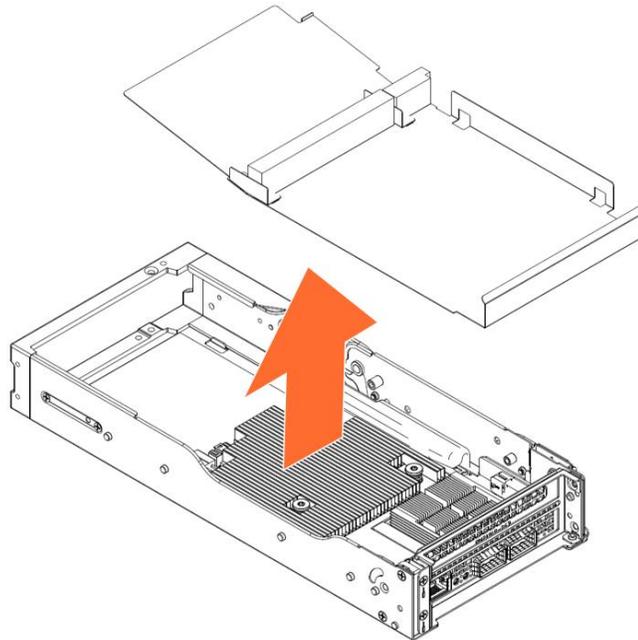
1. Disconnect the (1) BF3 NCSI signal cable, (2) MCIO connectors of the BF3 riser cable, and (3) BF3 Y power cable from the HPM board.



2. Use one hand to apply force with a tool (e.g. a scribe) to the latch on the switch board tray (the one above the middle PCIe tray) while using the other hand to pull the BF3 tray out of the system.



3. Remove the BF3 air duct from the BF3 tray.

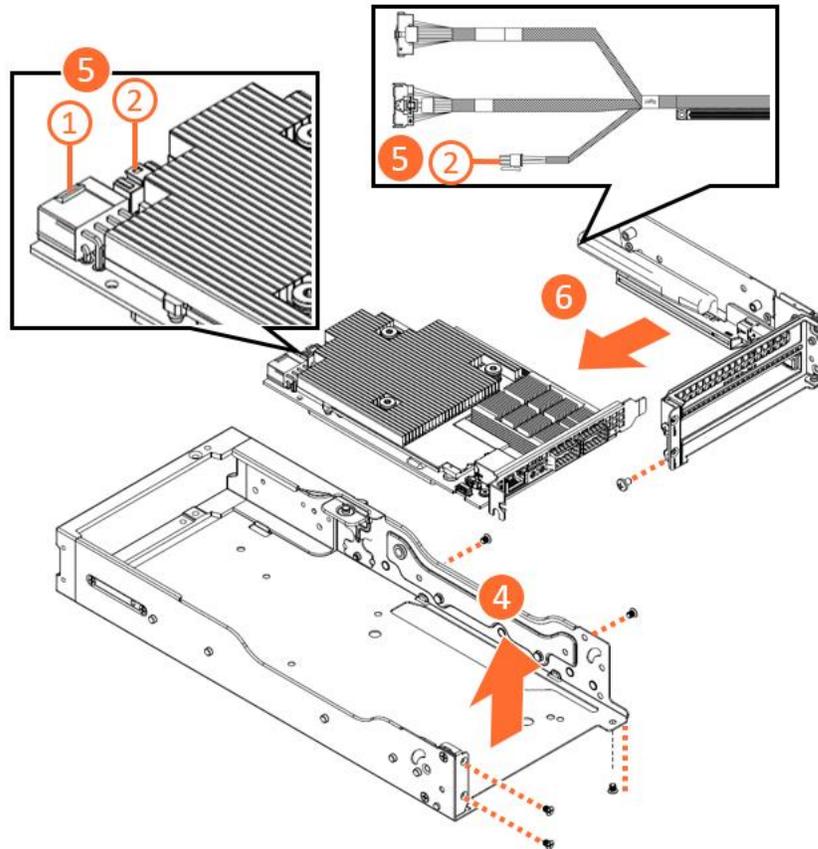


4. Remove five M3 screws securing the L-bracket to the BF3 tray and then remove the L-bracket with the BF3 card from the tray.
5. Disconnect and remove the (1) BF3 signal cable and (2) BF3 Y power cable from the BF3 card.

Note:

The BF3 Y power cable has one connector connected to the BF3 card and the other connector connected to the power connector of the riser cable that is pre-installed to the L-bracket, both of which must be disconnected.

6. Remove single M3 screw securing the BF3 card to the L-bracket and then separate the card from the bracket.



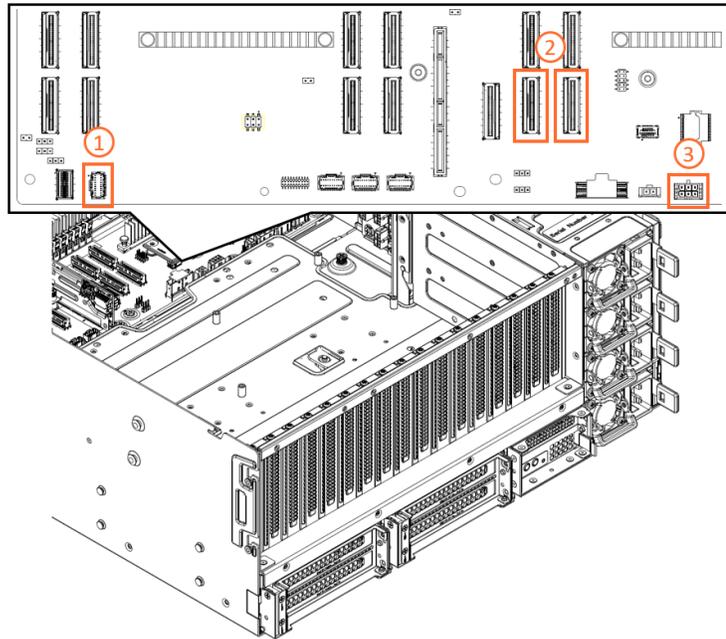
6.19.2 Installing the Add-On_2 Card

Prerequisites

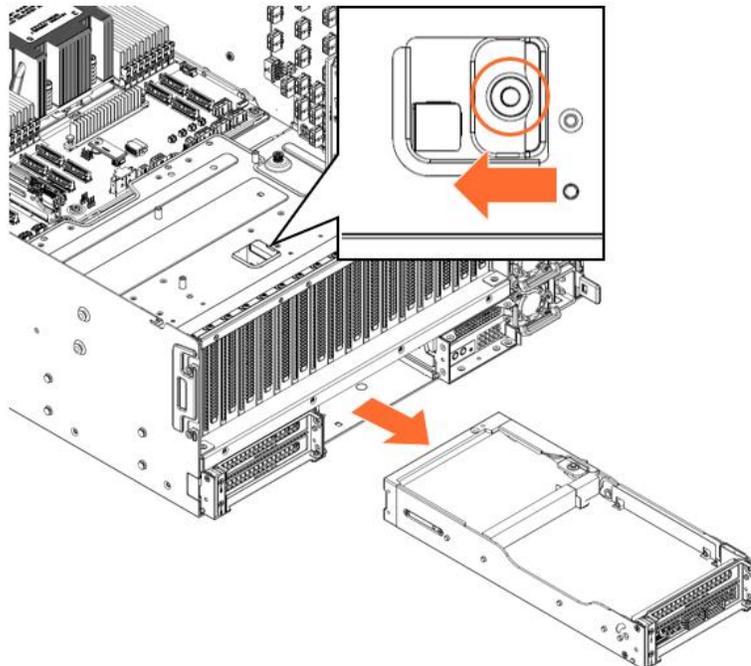
1. AC power off the system.
2. Remove Top Cover, GPU Card, GPU Card Support Bracket, Top Fan Cage Assembly, Air Duct, and Switch Daughter Board.

Steps

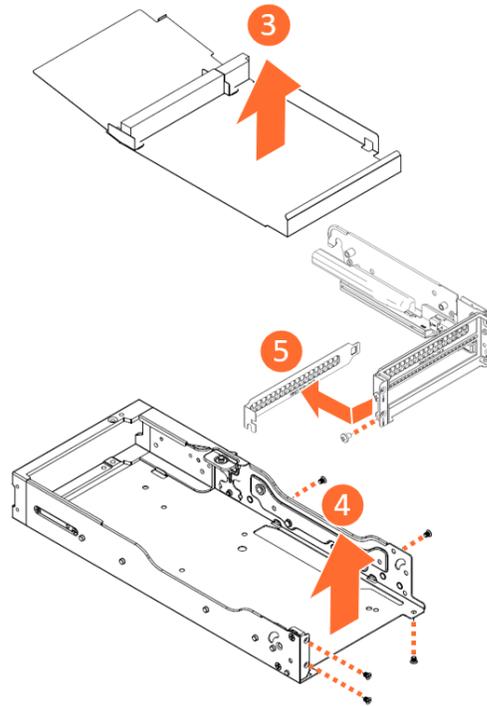
1. Disconnect the (1) BF3 NCSI signal cable, (2) MCIO connectors of the BF3 riser cable, and (3) BF3 Y power cable from the HPM board.



2. Use one hand to apply force with a tool (e.g. a scribe) to the latch on the switch board tray (the one above the middle PCIe tray) while using the other hand to pull the BF3 tray out of the system.



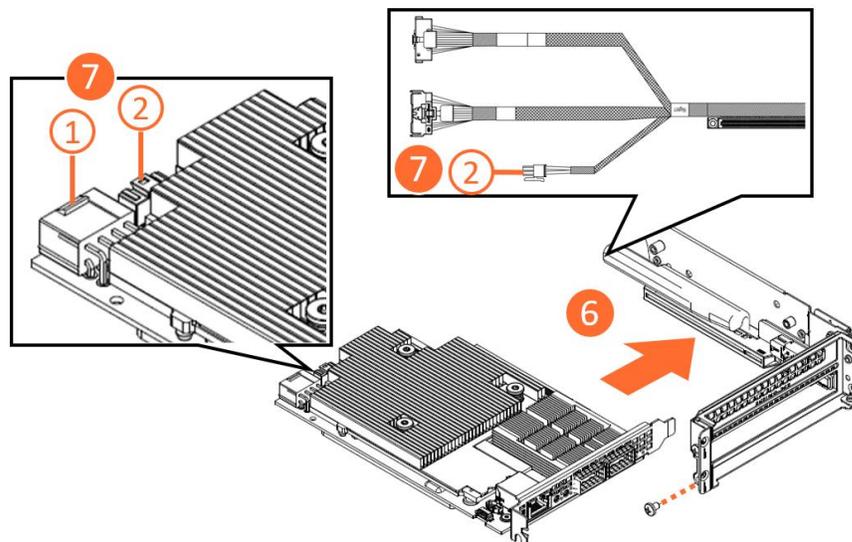
3. Remove the BF3 air duct from the BF3 tray.
4. Remove five M3 screws securing the L-bracket to the BF3 tray and then remove the L-bracket from the tray.
5. [For systems shipped without a BF3 card installed] Remove the single M3 screw securing the PCIe dummy bracket to the L-bracket and then remove the dummy bracket from the L-bracket.



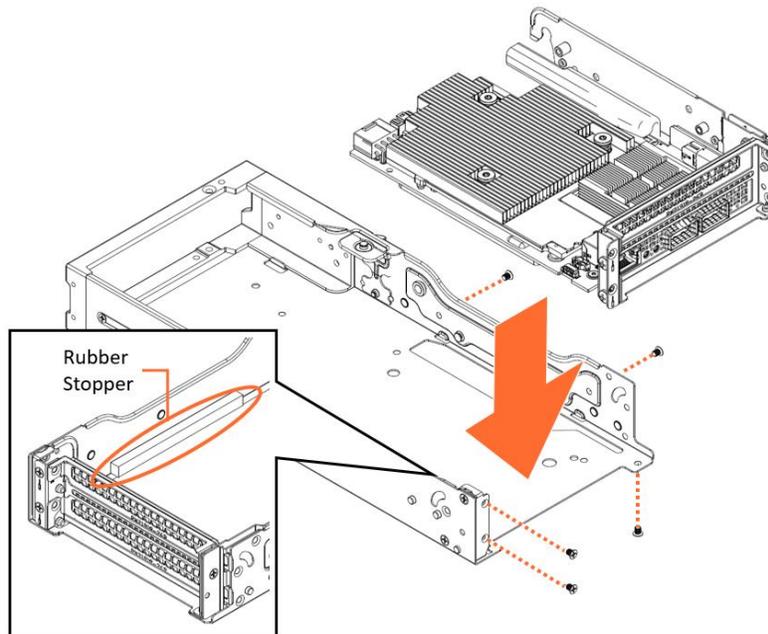
6. Insert the BF3 card into the riser cable connector on the L-bracket and install single M3 screw securing the BF3 card to the L-bracket (torque: 6 ± 0.5 kgf-cm).
7. Connect the (1) BF3 signal cable and (2) BF3 Y power cable to the BF3 card while threading the cable out of the rear opening of the tray.

Note:

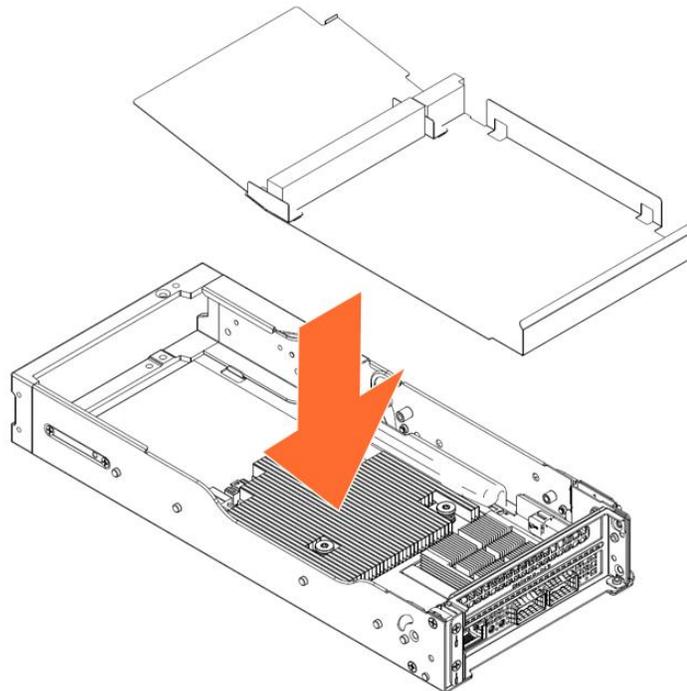
The BF3 Y power cable has two connectors. Connect one connector to the BF3 card and the other connector to the power connector of the riser cable that is pre-installed to the L-bracket.



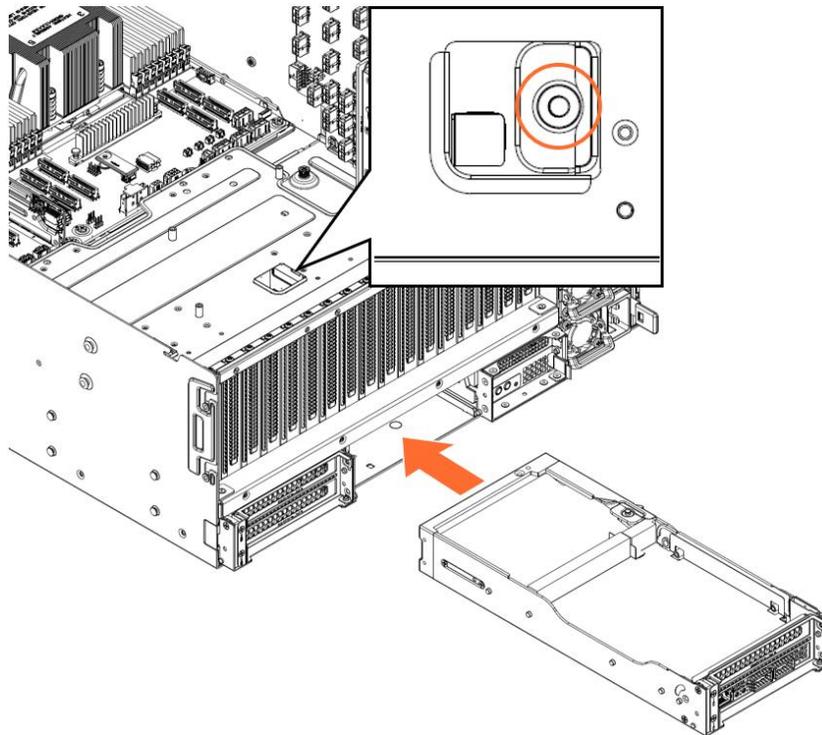
- Align the BF3 card against the rubber stopper on the PCIe tray and then install the BF3 card with the L-bracket assembly to the tray. Install five M3 screws to secure the assembly in place (torque: 6 ± 0.5 kgf-cm).



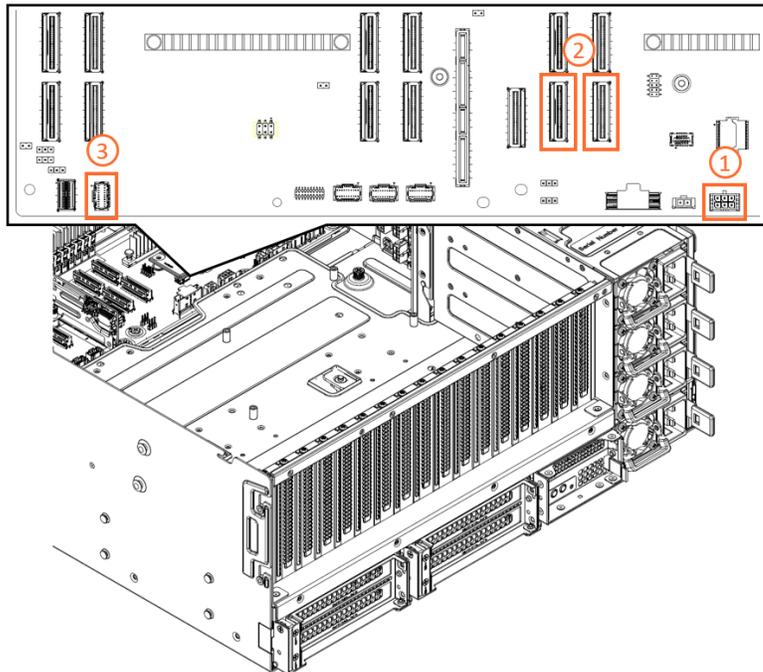
- Install the BF3 air duct back to the BF3 tray.



10. Install the BF3 tray back to the system. Ensure the latch is locked in place.



11. Connect the (1) BF3 Y power cable, (2) MCIO connector of the riser cable, and (3) BF3 NCSI signal cable to the HPM board.



Chapter 7 System Cable Routing

7.1 High-Speed Cables

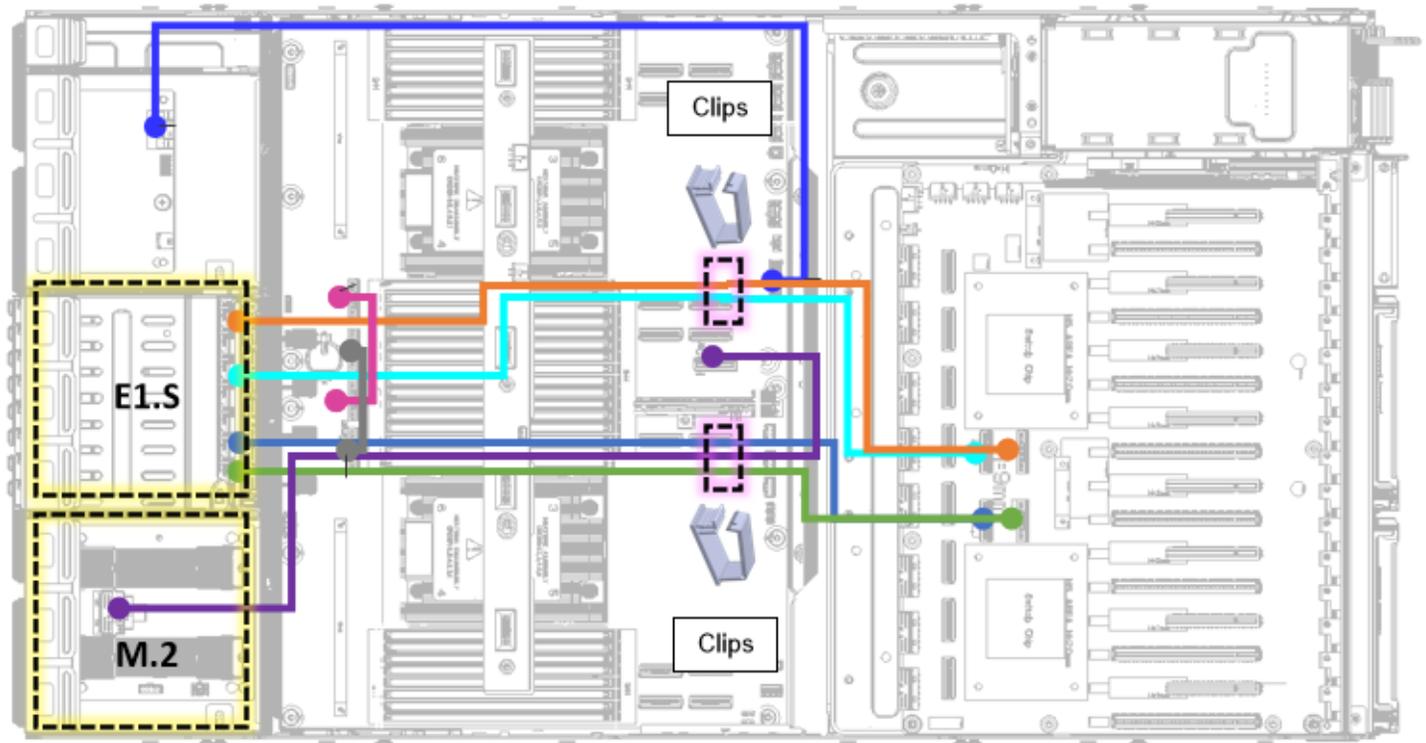


Figure 16. High Speed Cables (1/3)

Table 25. High Speed Cables (1/3)

Color Code	Description	From		To		From
		PCBA/Card	Pin Count	PCBA/Card	Pin Count	
	E1.S MCIO cable-1	E1.S BP	MCIOX8(RA)	Switch board	MCIOX8(VT)	1
	E1.S MCIO cable-2	E1.S BP	MCIOX8(RA)	Switch board	MCIOX8(VT)	1
	E1.S MCIO cable-3	E1.S BP	MCIOX8(RA)	Switch board	MCIOX8(VT)	1
	E1.S MCIO cable-4	E1.S BP	MCIOX8(RA)	Switch board	MCIOX8(VT)	1
	M.2 MCIO cable	M.2 board	MCIOX8	HPM board	MCIOX8	1
	XGMI MCIO cable-1	HPM board	MCIOX8	HPM board	MCIOX8	1
	XGMI MCIO cable-2	HPM board	MCIOX8	HPM board	MCIOX8	1
	Front IO Slim SAS cable	Front IO board	Slim SAS X8	HPM board	Slim SAS X8	1

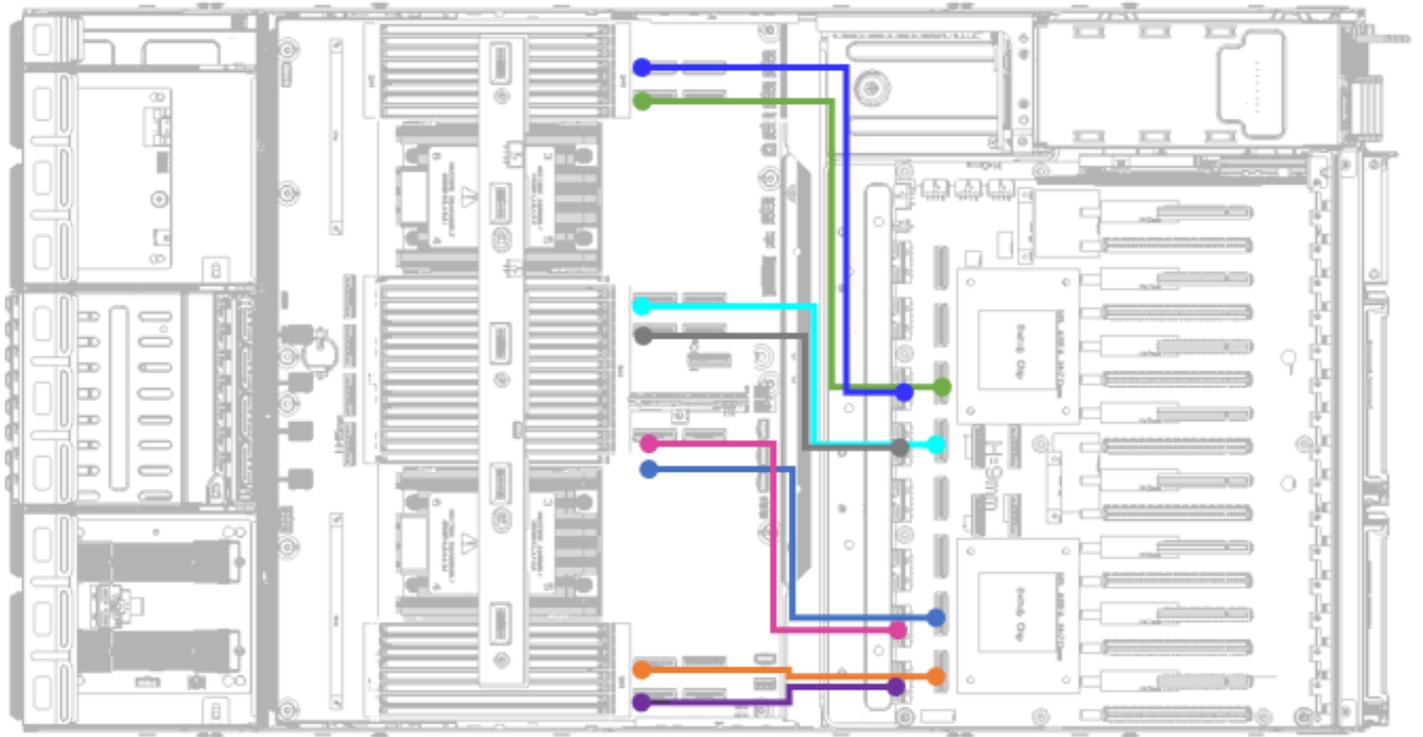


Figure 17. High Speed Cables (2/3)

Table 26. High Speed Cables (2/3)

Color Code	Description	From		To		From
		PCBA/Card	Pin Count	PCBA/Card	Pin Count	
	Switch MCIO cable-R1	Switch board	MCIOX8(RA)	HPM board	MCIOX8(VT)	1
	Switch MCIO cable-R2	Switch board	MCIOX8(RA)	HPM board	MCIOX8(VT)	1
	Switch MCIO cable-R3	Switch board	MCIOX8(RA)	HPM board	MCIOX8(VT)	1
	Switch MCIO cable-R4	Switch board	MCIOX8(RA)	HPM board	MCIOX8(VT)	1
	Switch MCIO cable-V1	Switch board	MCIOX8(VT)	HPM board	MCIOX8(VT)	1
	Switch MCIO cable-V2	Switch board	MCIOX8(VT)	HPM board	MCIOX8(VT)	1
	Switch MCIO cable-V3	Switch board	MCIOX8(VT)	HPM board	MCIOX8(VT)	1
	Switch MCIO cable-V4	Switch board	MCIOX8(VT)	HPM board	MCIOX8(VT)	1

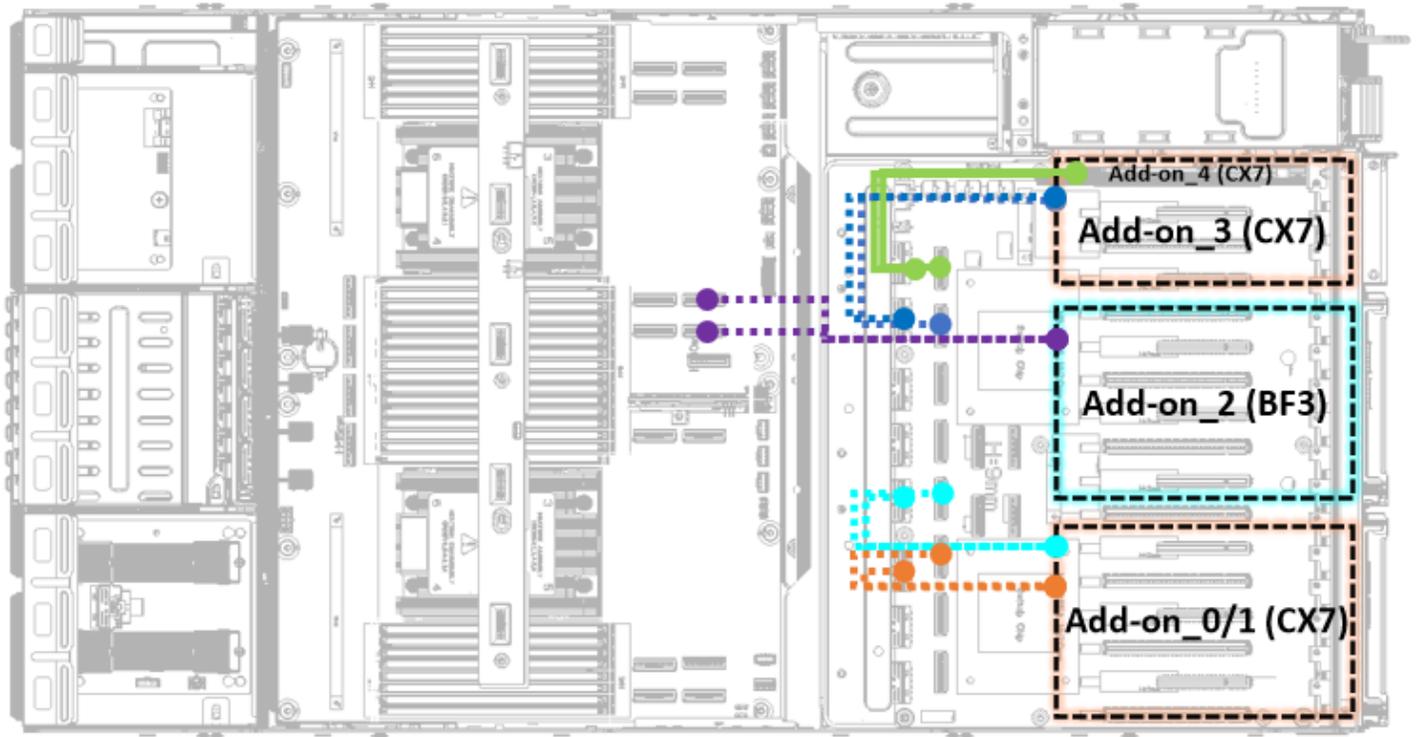


Figure 18. High Speed Cables (3/3)

Table 27. High Speed Cables (3/3)

Color Code	Description	From		To		From
		PCBA/Card	Pin Count	PCBA/Card	Pin Count	
	CX7 CEM Riser cable-1	CX7 device	PCIeX16	Switch board	MCIOX8*2	1
	CX7 CEM Riser cable-2	CX7 device	PCIeX16	Switch board	MCIOX8*2	1
	CX7 CEM Riser cable-3	CX7 device	PCIeX16	Switch board	MCIOX8*2	1
	CX7 SW CEM Riser cable	CX7 device	PCIeX16	Switch board	MCIOX8*2	1
	BF3 CEM Riser cable	BF3 device	PCIeX16	HPM board	MCIOX8*2	1

7.2 Power Cables

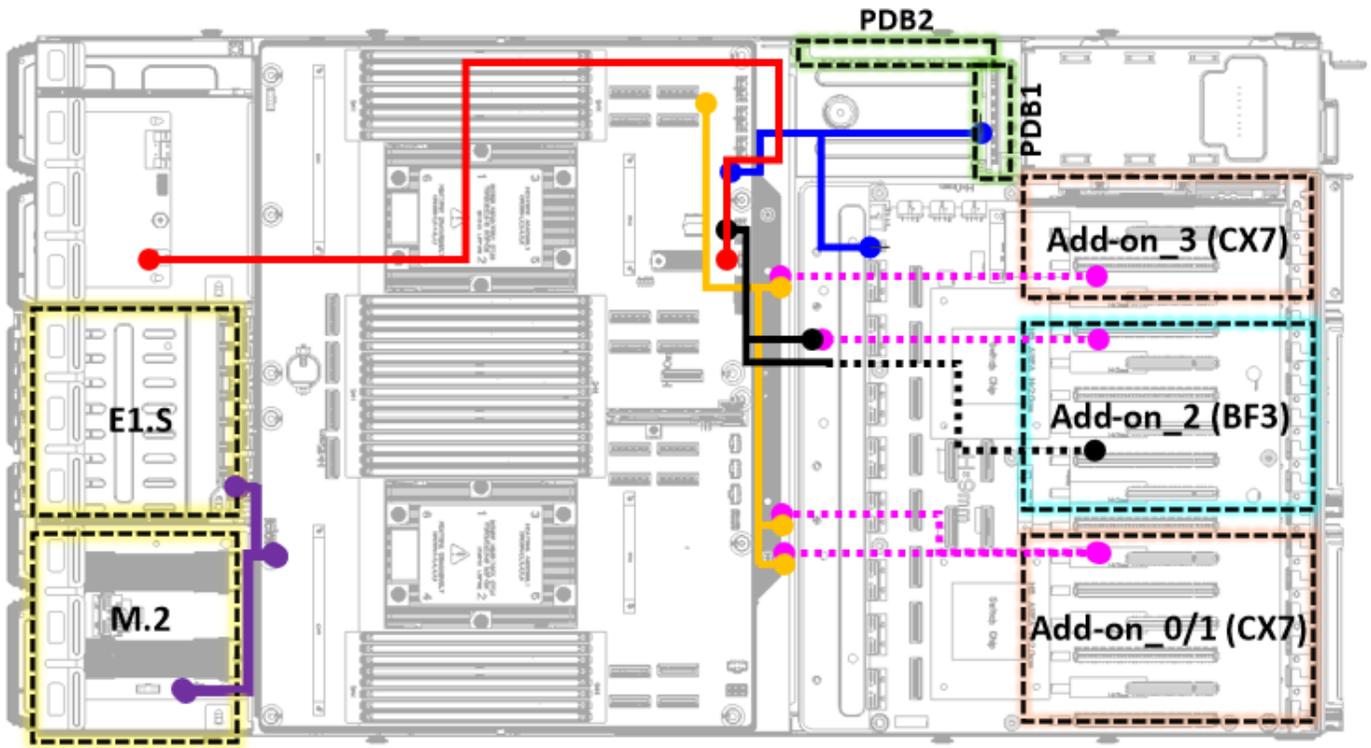


Figure 19. Power Cables (1/6)

Table 28. Power Cables (1/6)

Color Code	Description	From		To		From
		PCBA/Card	Pin Count	PCBA/Card	Pin Count	
	CX7 Riser cable (power)	CX7	2X2P	C6 cable	2X2P	3
	BF3 Riser cable (power)	BF3	2X2P	C30 cable	2X2P	1
	Riser power switch cable	C1,2,3 cable	3*2X2P	HPM board	2X4P	1
	M.2/E1.S BP power cable	E1.S/ BP	2*2X2P	HPM board	2X4P	1
	Front IO power cable	Front IO	1X2P	HPM board	1X2P	1
	MB/SW Y power cable	PDB1	2X2P	MB/SW	2*1X2P	1
	BF3 Y power cable	BF3/riser cable	8P PH4.2/4P	HPM board	2X3P	1

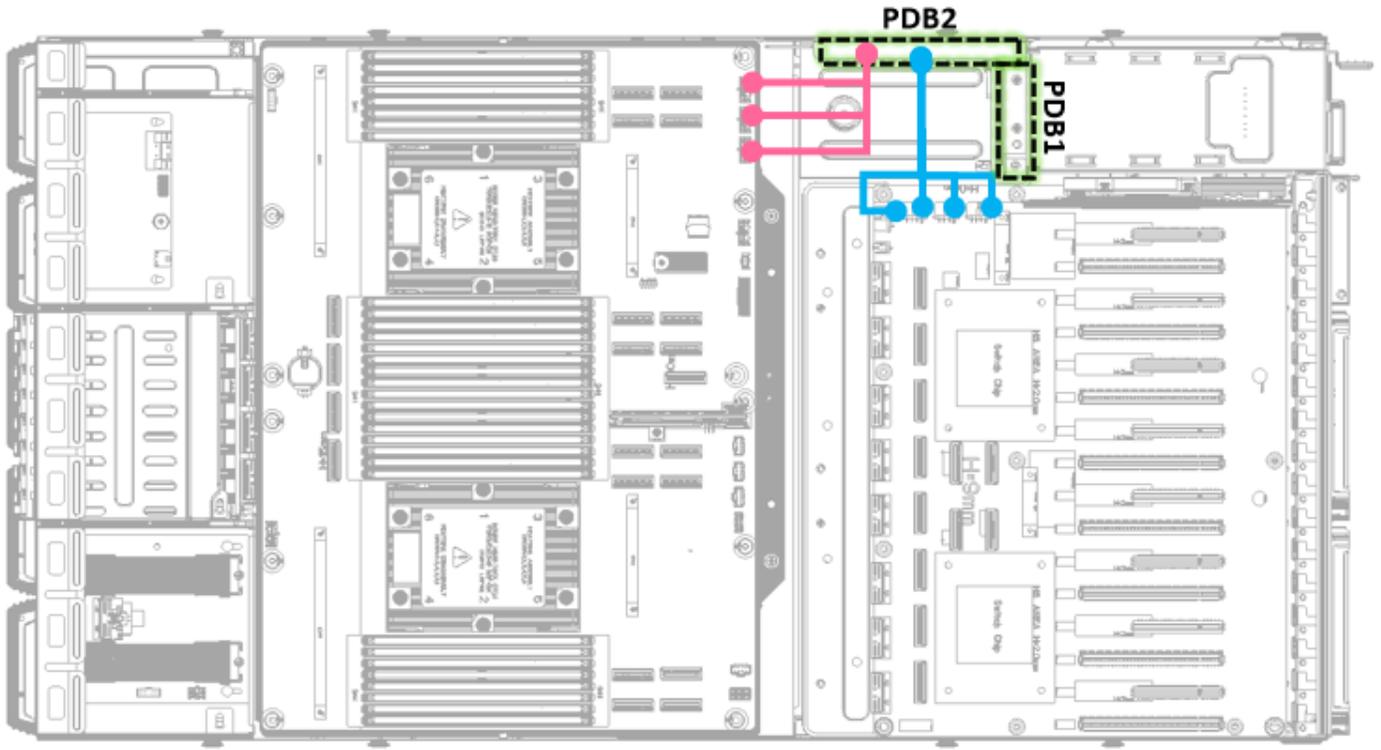


Figure 20. Power Cables (2/6)

Table 29. Power Cables (2/6)

Color Code	Description	From		To		Qty/ Set
		PCBA/Card	Pin Count	PCBA/Card	Pin Count	
	Switch power cable(8P)	Switch board	2X4P	PDB2	2X4P	4
	MB power cable	PDB2	2X4P	HPM board	2X4P	3

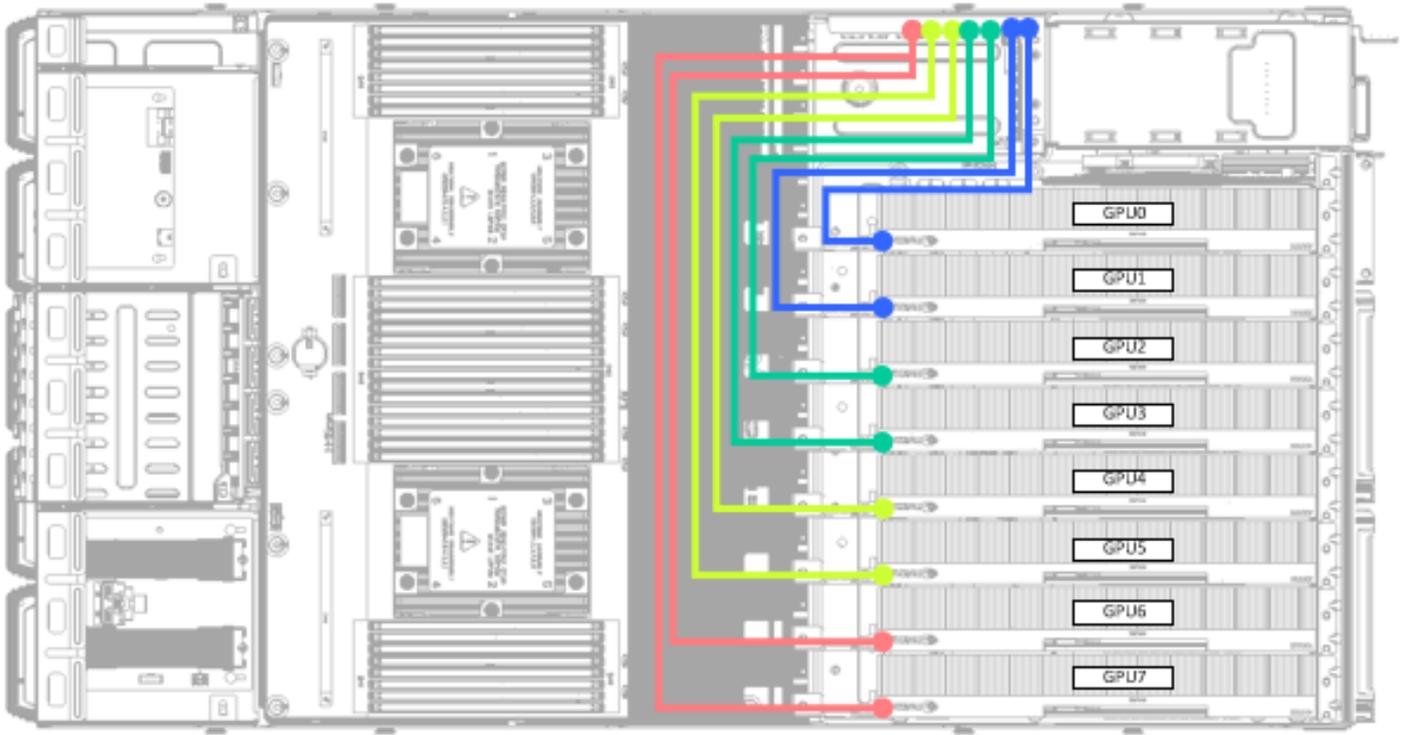


Figure 21. Power Cables (3/6)

Table 30. Power Cables (3/6)

Color Code	Description	From		To		Qty/ Set
		PCBA/Card	Pin Count	PCBA/Card	Pin Count	
	GPU power cable(600W)-1	GPU device	12P+4S	PDB2	2X4P	2
	GPU power cable(600W)-2	GPU device	12P+4S	PDB2	2X4P	2
	GPU power cable(600W)-3	GPU device	12P+4S	PDB2	2X4P	2
	GPU power cable(600W)-4	GPU device	12P+4S	PDB2	2X4P	2

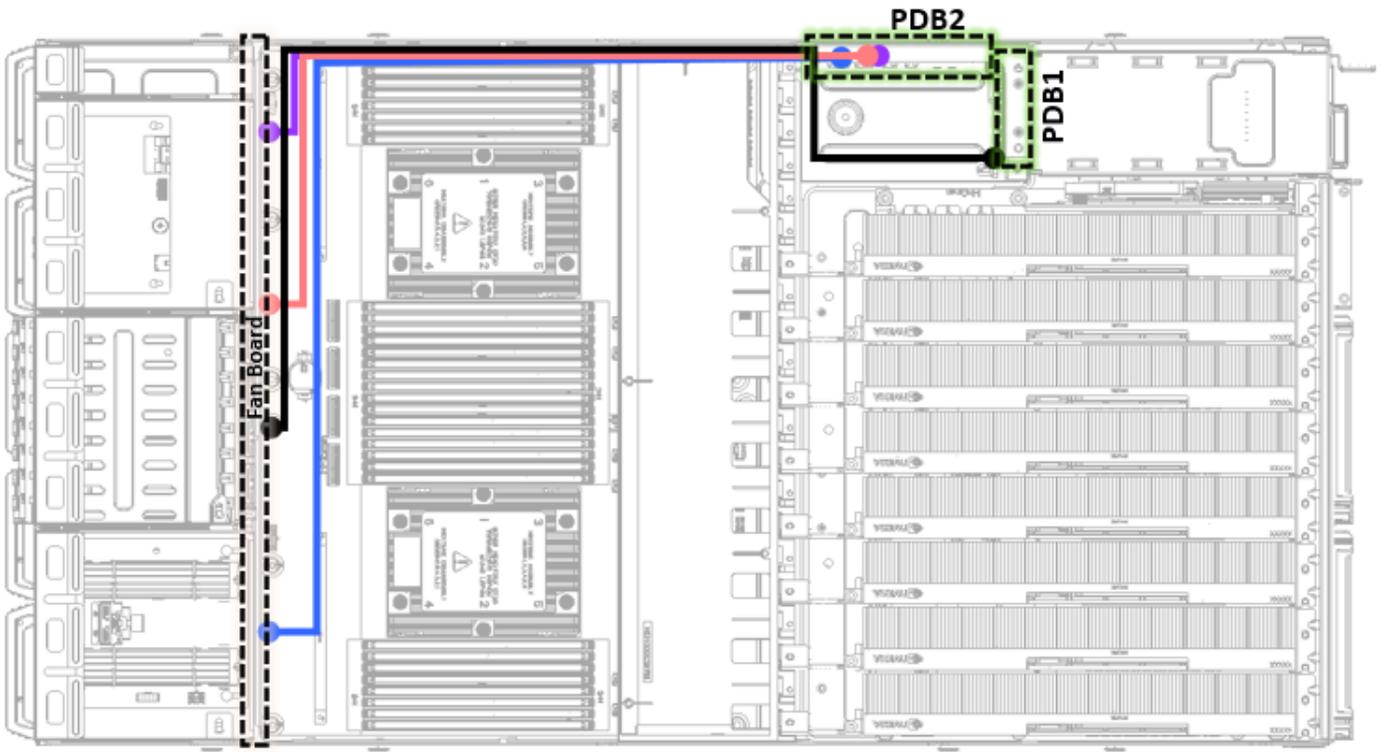


Figure 22. Power Cables (4/6)

Table 31. Power Cables (4/6)

Color Code	Description	From		To		Qty/ Set
		PCBA/Card	Pin Count	PCBA/Card	Pin Count	
	PDB1 fan power cable(2P)	PDB1	1X8P	Fan RA board	1X2P	1
	Fan power cable-RA(10P)	RA Fan board	2X5P	PDB2	2X5P	1
	Fan power cable-RA1(8P)	RA Fan board	2X4P	PDB2	2X4P	1
	Fan power cable-RA2(8P)	RA Fan board	2X4P	PDB2	2X4P	1

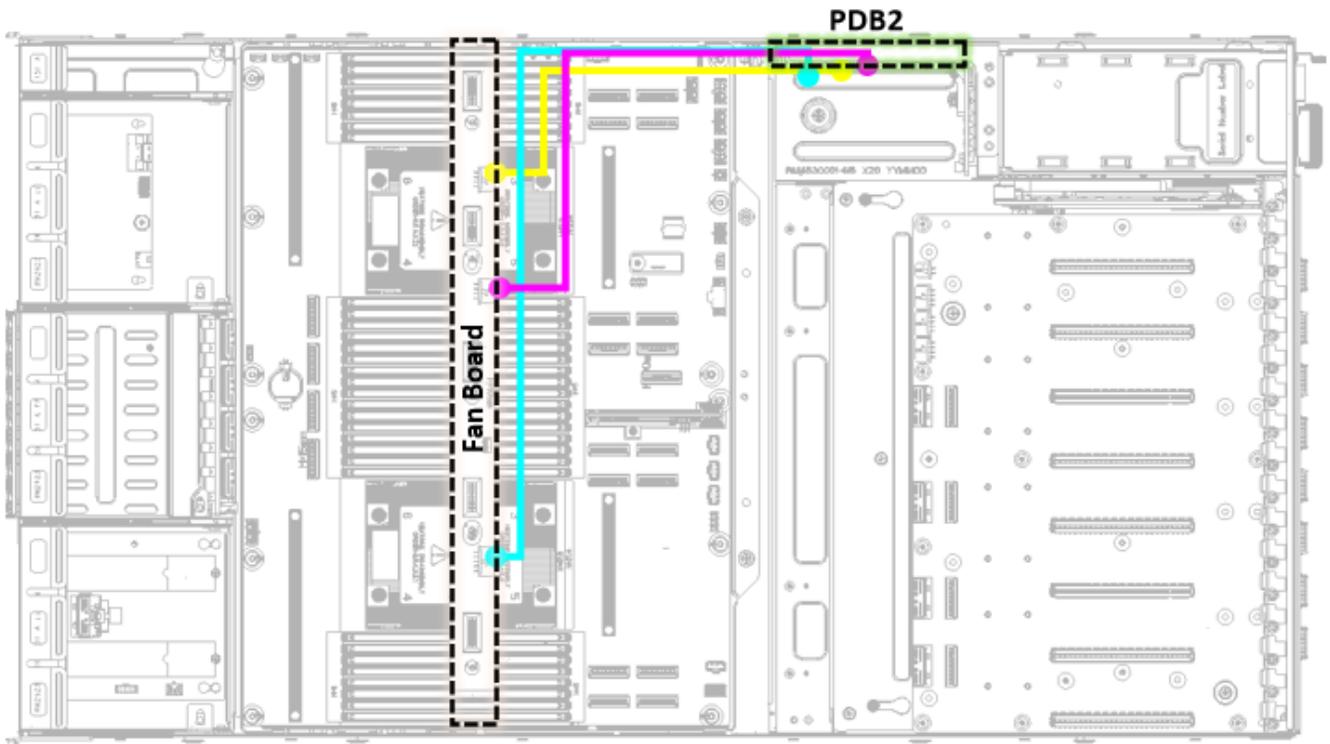


Figure 23. Power Cables (5/6)

Table 32. Power Cables (5/6)

Color Code	Description	From		To		Qty/ Set
		PCBA/Card	Pin Count	PCBA/Card	Pin Count	
	Fan power cable-VT(10P)	VT Fan board	2X5P	PDB2	2X5P	1
	Fan power cable-VT1(8P)	VT Fan board	2X4P	PDB2	2X4P	1
	Fan power cable-VT2(8P)	VT Fan board	2X4P	PDB2	2X4P	1

7.3 Signal Cables



Figure 24. Signal Cables

Table 33. Signal Cables

Color Code	Description	From		To		Qty/ Set
		PCBA/Card	Pin Count	PCBA/Card	Pin Count	
	BF3 NCSI signal cable	BF3	20P	HPM board	20P	1
	Rear IO sideband cable	Rear IO	2X6P	HPM board	2X6P	1
	Fan signal cable-RA	Fan board	1X8P	HPM board	1X8P	1
	Fan signal cable-VT	Fan board	1X8P	HPM board	1X8P	1
	PDB1 sideband cable	PDB1	20P	HPM board	20P	1
	M.2 sideband cable	M.2	1X4P	HPM board	1X4P	1
	E1.S BP sideband cable	BP	1X4P	HPM board	1X4P	1

Chapter 8 POST Process and BIOS Setup

The system supports the following operating systems:

Table 34. Supported Operating Systems

Operation System	Version
Ubuntu	Ubuntu 22.04 LTS or later
Red Hat Enterprise Linux (RHEL)	RHEL 9.2 or later
Windows Server	Windows Server 2022 or later

8.1 POST Process

Follow the steps below to complete the POST process:

1. Starting the POST Process

After power-on, a PEGATRON SVR logo will appear indicating the POST process has started. The logo will be displayed for several minutes until the system is ready for the **early POST** stage.



Figure 25. Starting the POST Process

2. Initializing BMC

The BMC-initializing screen will be displayed when the system enters early POST.



Figure 26. Early POST- BMC Initializing

3. Once BMC initialization is completed, the Screen Information screen will be displayed, showing information about the BMC version, port 80 status, CPU, etc.

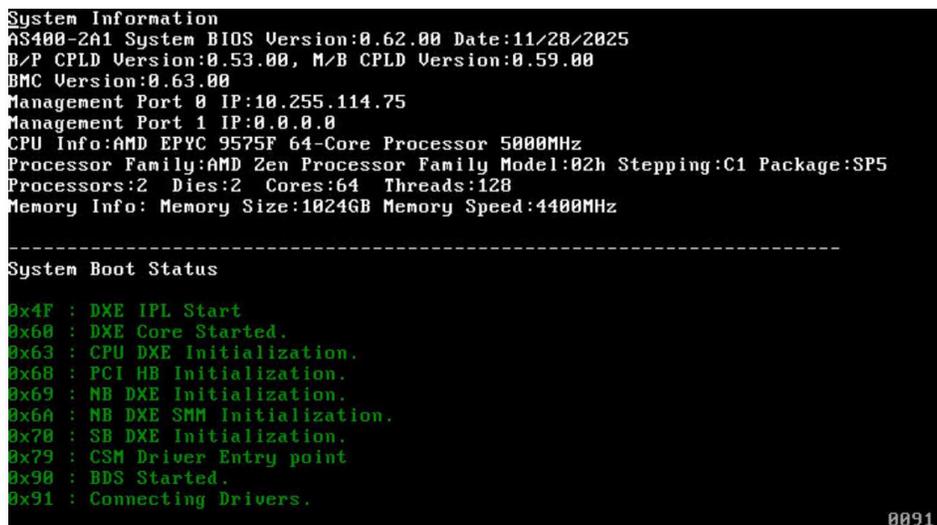


Figure 27. Early POST - System Information

4. After the early POST, the following diagnostic screen will be displayed indicating the system is running the self-test. Wait a few minutes and the system will automatically proceed.

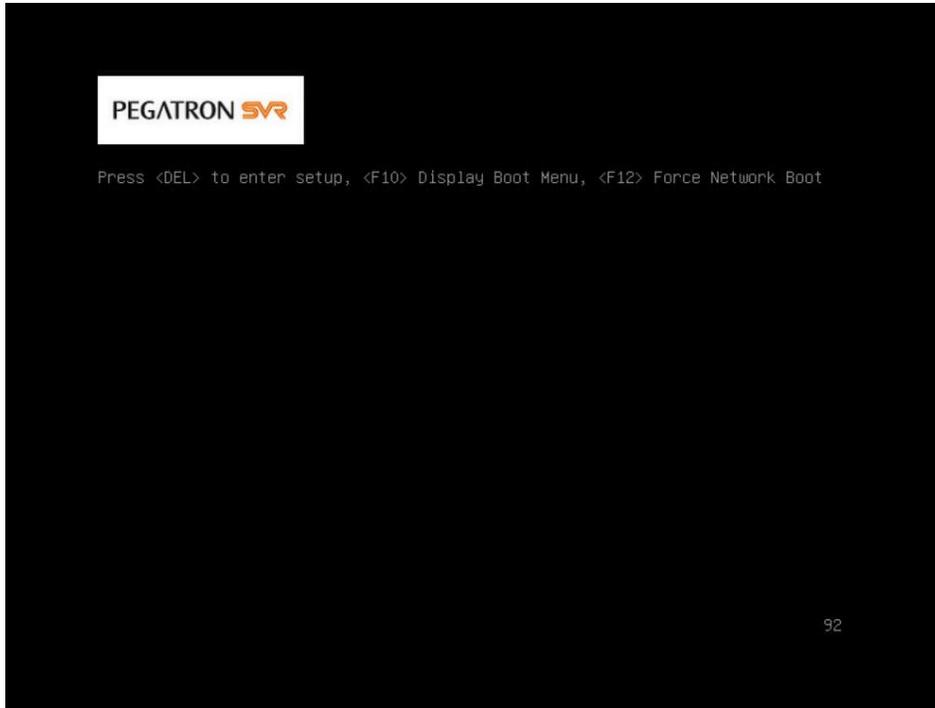


Figure 28. BIOS Diagnostic Screen

5. When the self-test is completed, the system will display diagnostic information and import firmware configuration settings.

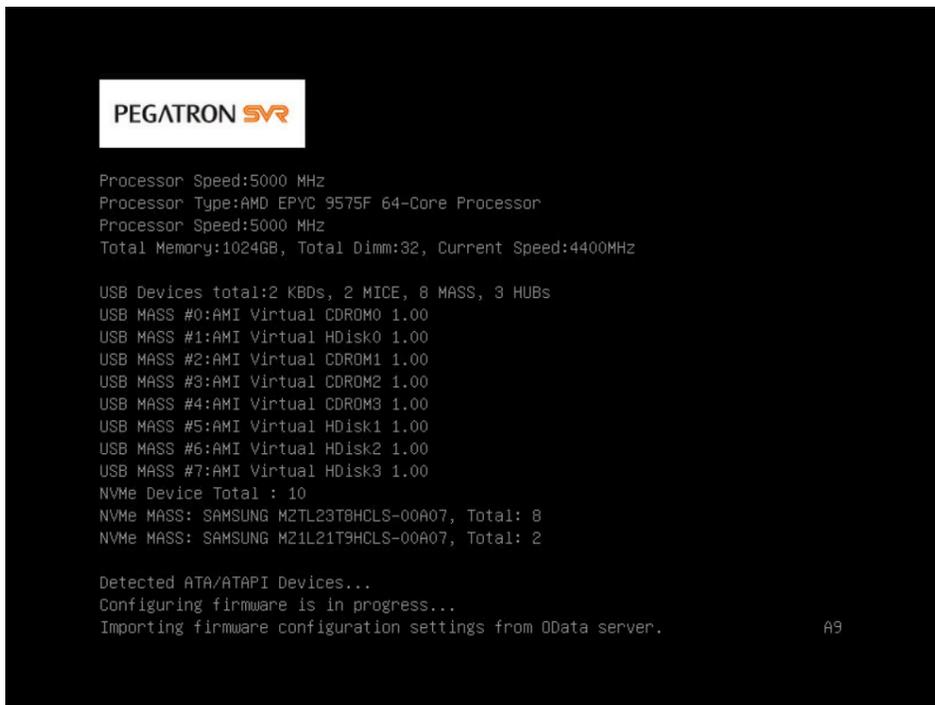


Figure 29. BIOS Diagnostic Information Screen

Note:

If the following warning message appears on the diagnostic information screen, it means that the system may have problems that require action. Please download the system event log from the BMC web interface or the Redfish interface for further analysis.

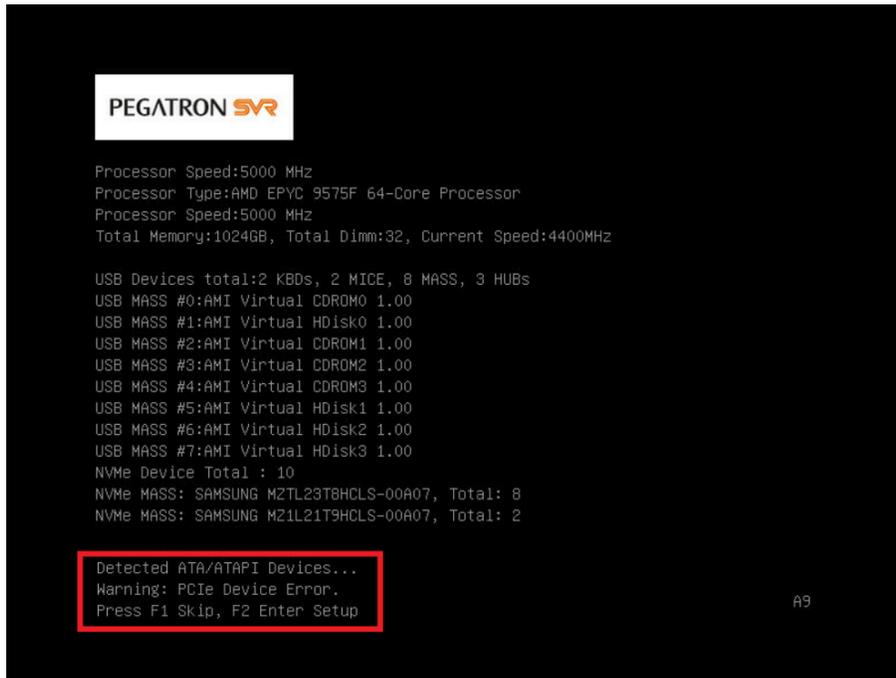


Figure 30. BIOS Diagnostic Screen - Warning Message

- When the firmware configuration settings are imported, the following screen will be displayed indicating the POST process is completed.

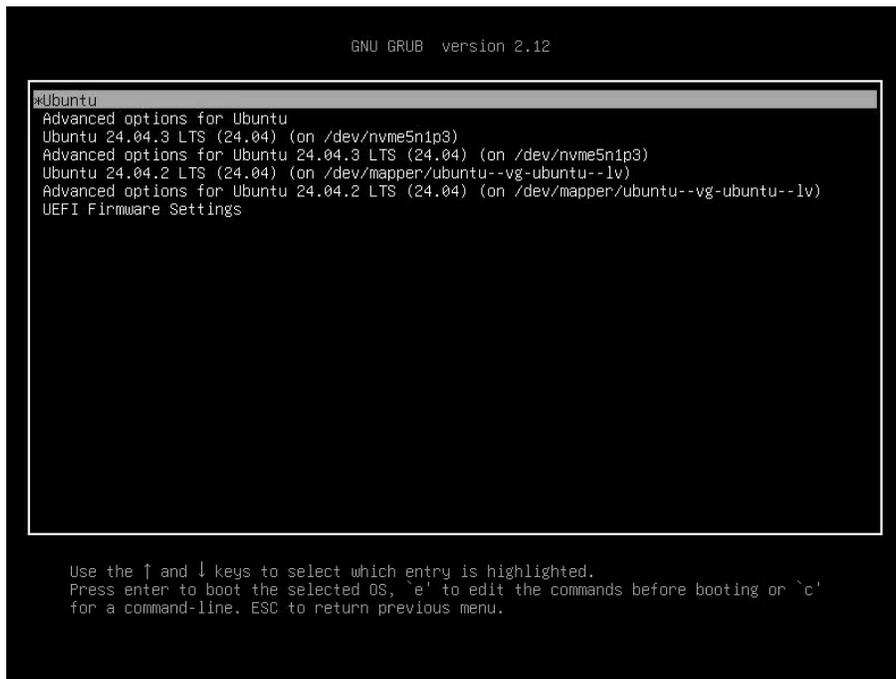


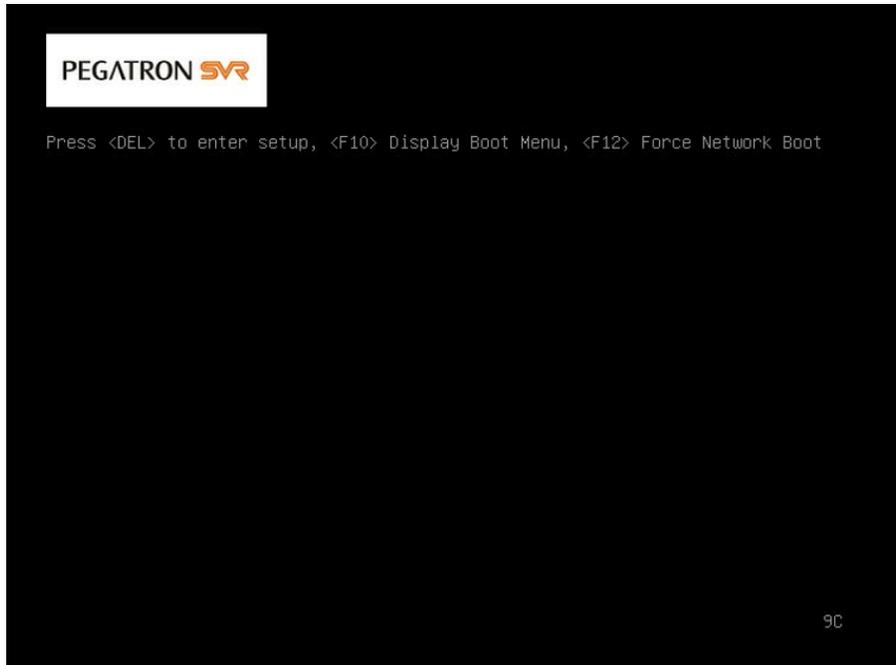
Figure 31. POST Process Completed

8.2 BIOS Setup Menu

8.2.1 Entering the BIOS Setup Menu

To enter the BIOS setup menu:

1. Follow steps 1 to 4 in section 8.1 **POST Process** to enter the diagnostic screen:



2. Press the **DEL** key to enter the BIOS Setup Menu. If the action is successfully triggered, the screen will display the "Enter Setup..." message.

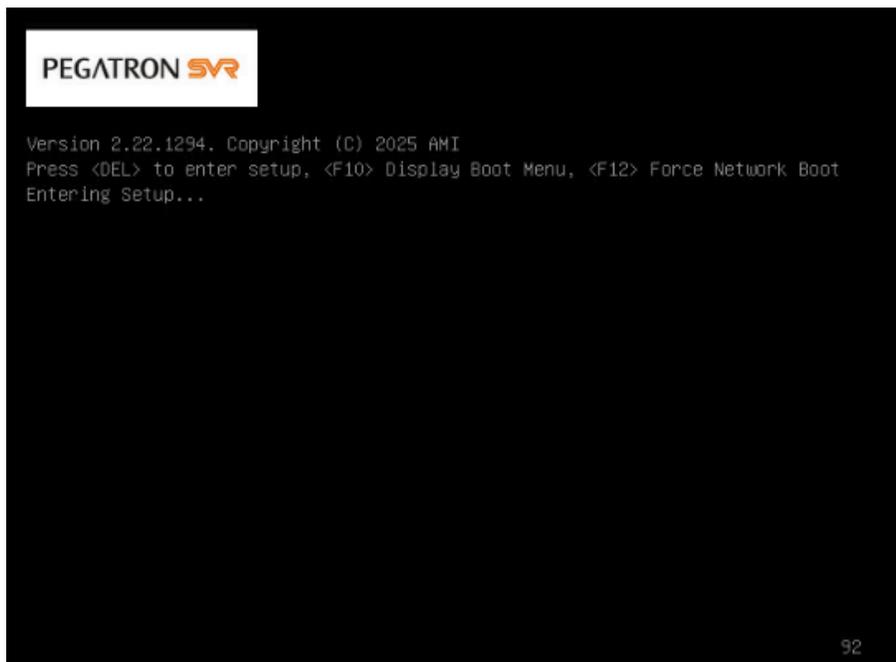


Figure 32. Entering the BIOS Setup Menu

8.2.2 BIOS Setup Menu

The Setup Menu consists of several tab pages; each provides access to different categories of configuration options:

Main

The Main page displays basic device information such as BIOS version, processor details, and memory configuration. It also allows date and time settings that are synchronized with the OS date and time.

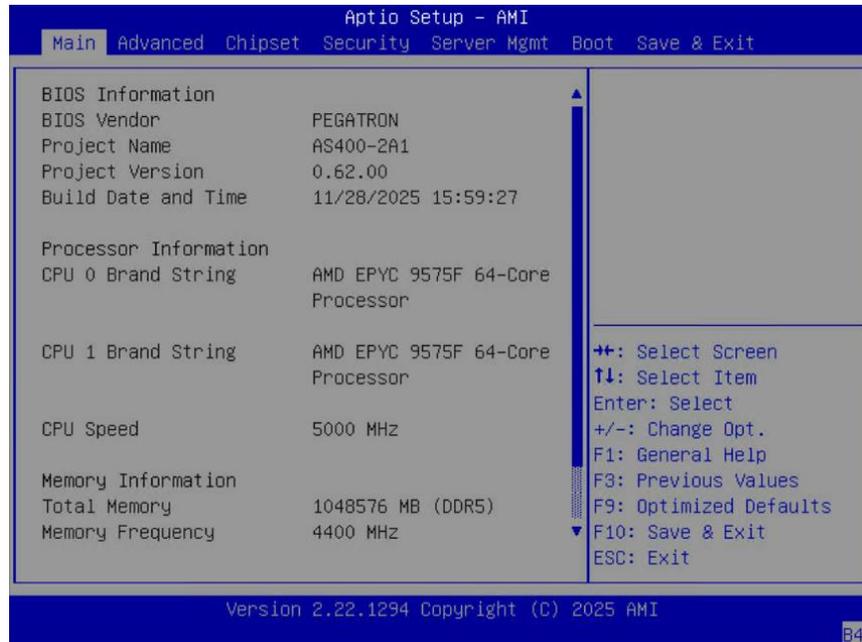


Figure 33. BIOS Setup Menu - Main Page

Advanced

The Advanced page offers access to a variety of detailed configuration options for system features. Individual parameters are organized within dedicated submenus.

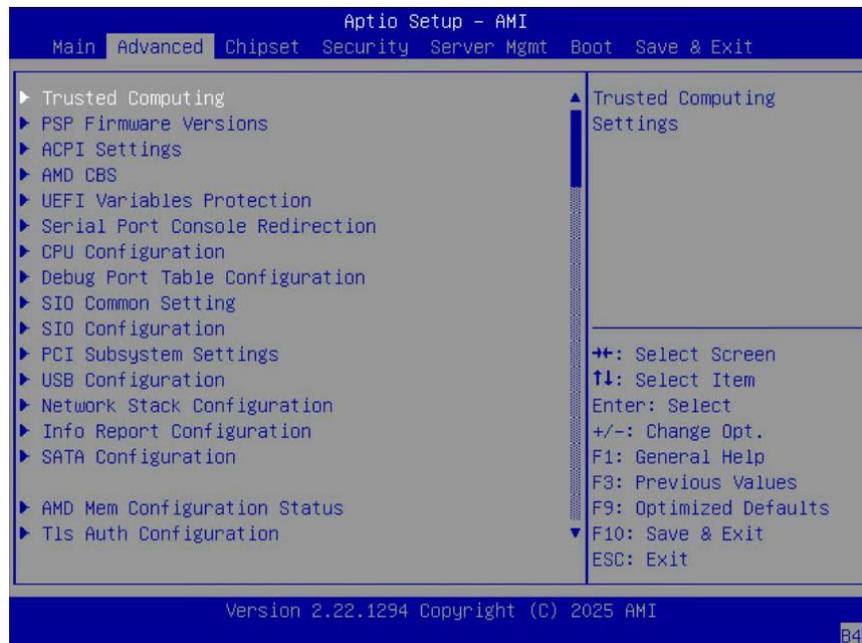


Figure 34. BIOS Setup Menu - Advanced Page

Chipset

The Chipset page allows configuring the functions related to the system chipset.



Figure 35. BIOS Setup Menu - Chipset Page

Security

The Security page allows management of user privileges and device security settings, including password protection and secure boot features.

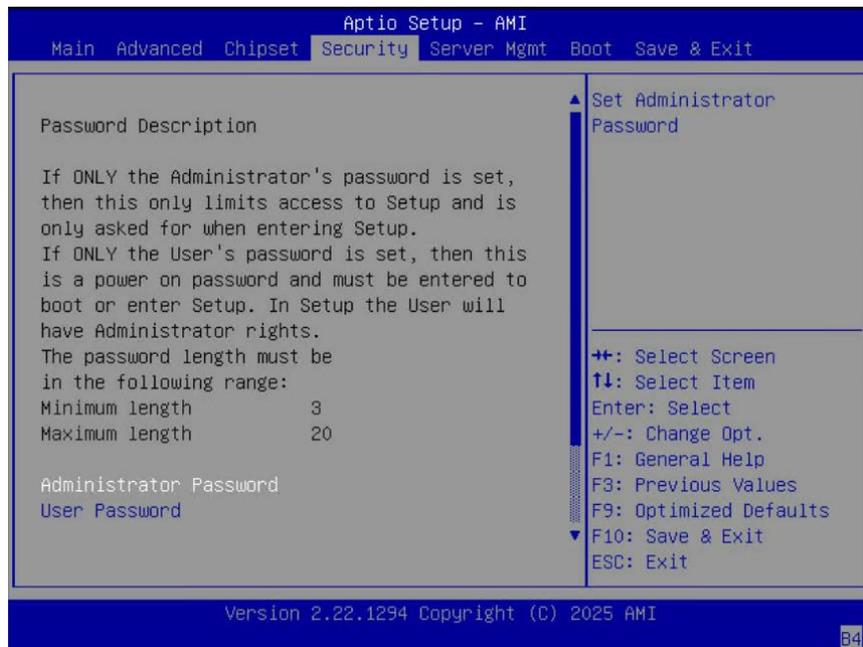


Figure 36. BIOS Setup Menu - Security Page

Server Management

The Server Mgmt page displays BMC information and allows BMC related settings.

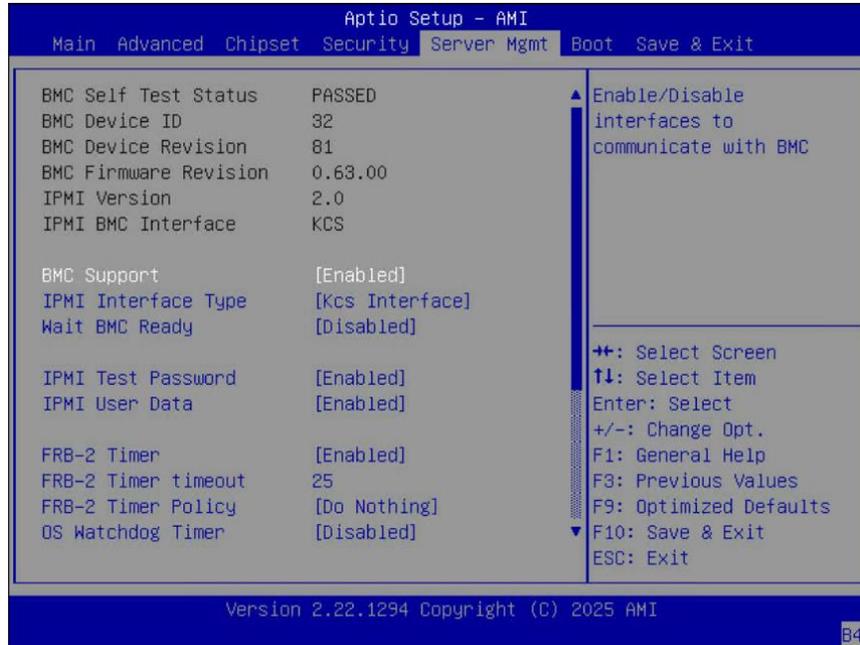


Figure 37. BIOS Setup Menu - Server Mgmt page

Boot

The Boot page displays bootable media encountered during the POST phase and allows users to configure boot sequence and boot priority for available boot devices.

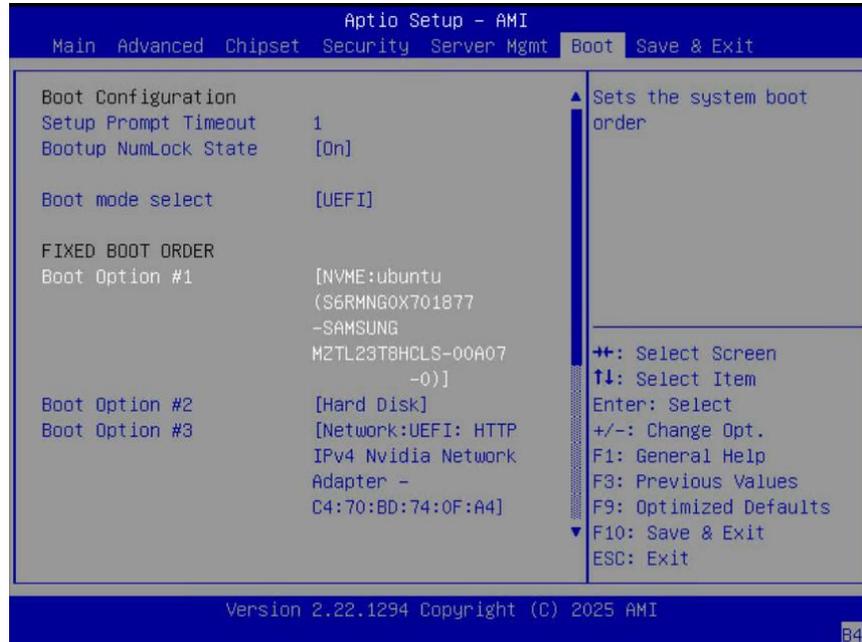


Figure 38. BIOS Setup Menu - Boot Page

Save & Exit

The Save & Exit page allows users to choose whether to save or discard the changes made to parameter options on other pages. It also allows users to restore the manufacturer default values and select boot devices before exiting the Setup menu.

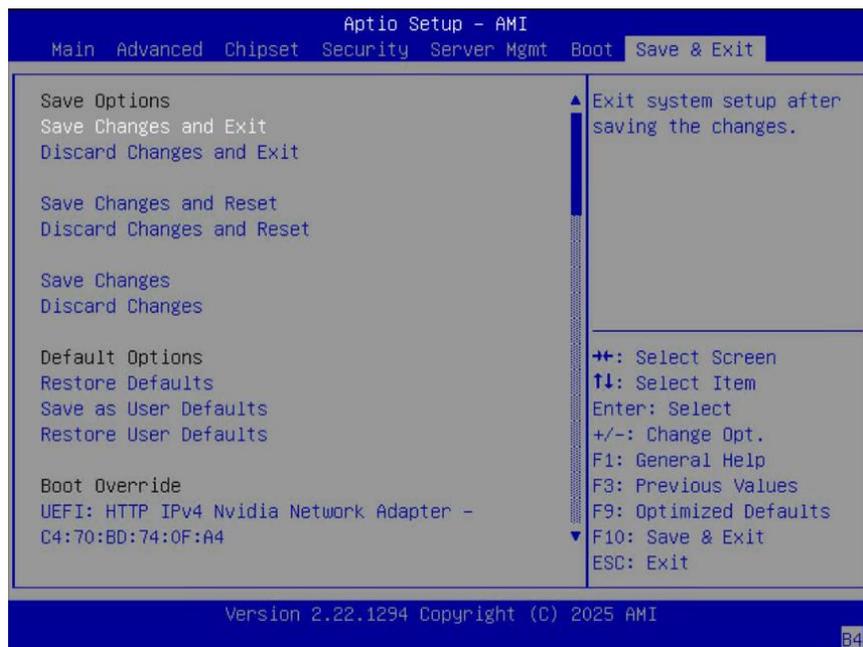


Figure 39. BIOS Setup Menu - Save & Exit Page

8.2.3 Option ROM

PCIe devices with Option ROM support are collectively listed under the Advanced page regardless of device type.

For example, an NVMe device that includes Option ROM support will be listed in the Advanced menu as below picture.

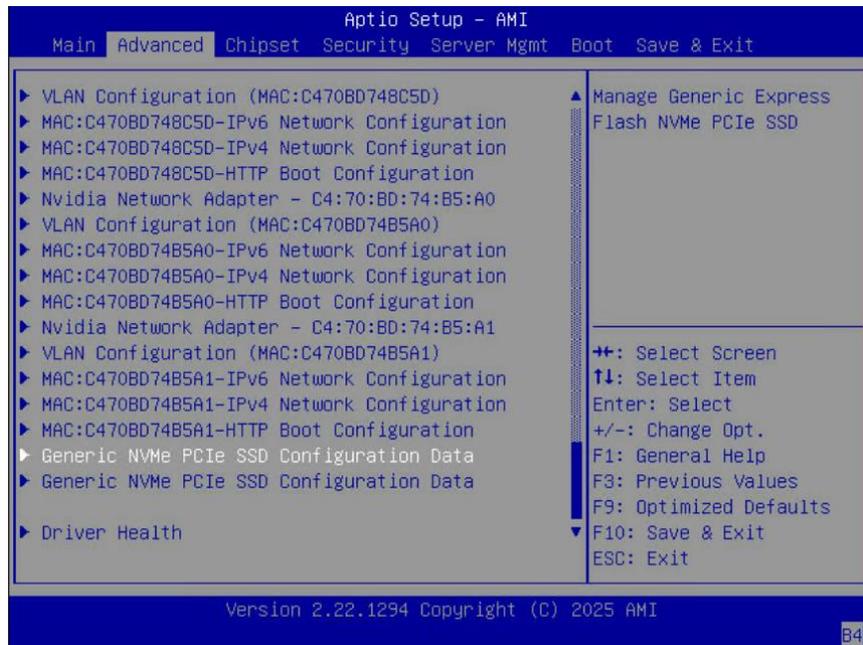


Figure 40. Advanced page – Devices with Option ROM

NVMe Devices without Option ROM support will appear under the NVMe Configuration page instead.



Figure 41. NVMe Configuration page – NVMe without Option ROM

8.2.4 BMC IP Setup

Follow the steps below to set up or confirm the BMC IP address (Management IP) in the BIOS Setup:

1. Follow the instructions in the **Entering the BIOS Setup Menu** section to enter the BIOS setup menu.
2. Select **“BMC network configuration”** under the **“Server Mgmt”** tab.

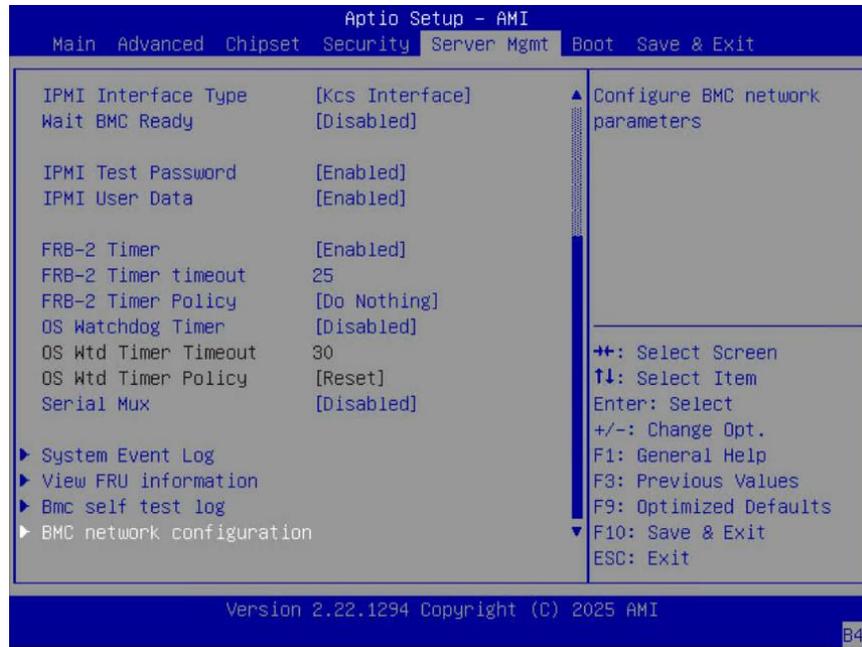


Figure 42. BIOS – BMC Network Configuration

3. Select a method of obtaining an IP address as needed (**Unspecified**, **Static**, **DynamicBmcDhcp**, or **DynamicBmcNonDhcp**).

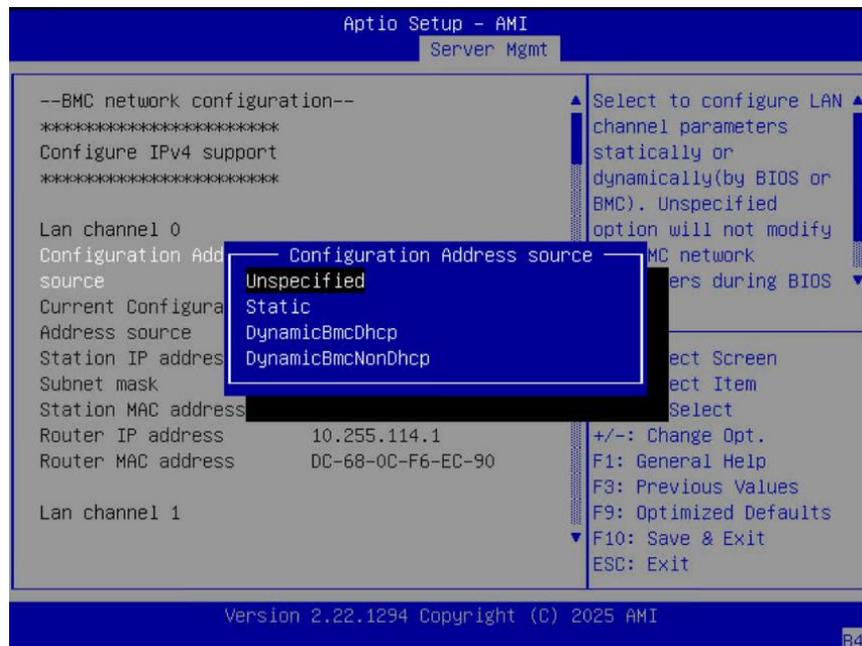


Figure 43. BIOS – BMC IP Configuration Source

If you want to use a dynamic IP address, select **DynamicBmcDhcp** (Dynamic BMC DHCP) and the DHCP server will dynamically assign an IP for your server system; the assigned IP will be displayed in the **Station IP address** row.

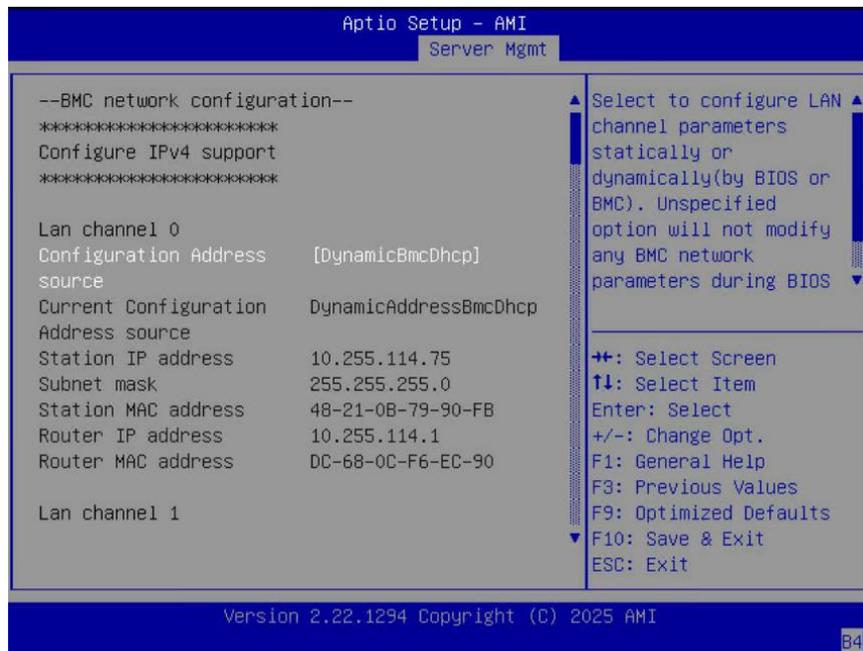


Figure 44. BIOS – BMC DHCP IP Configuration

If you want to use a static IP, select **Static** and fill in your static IP address in the **Station IP address** window that appears.

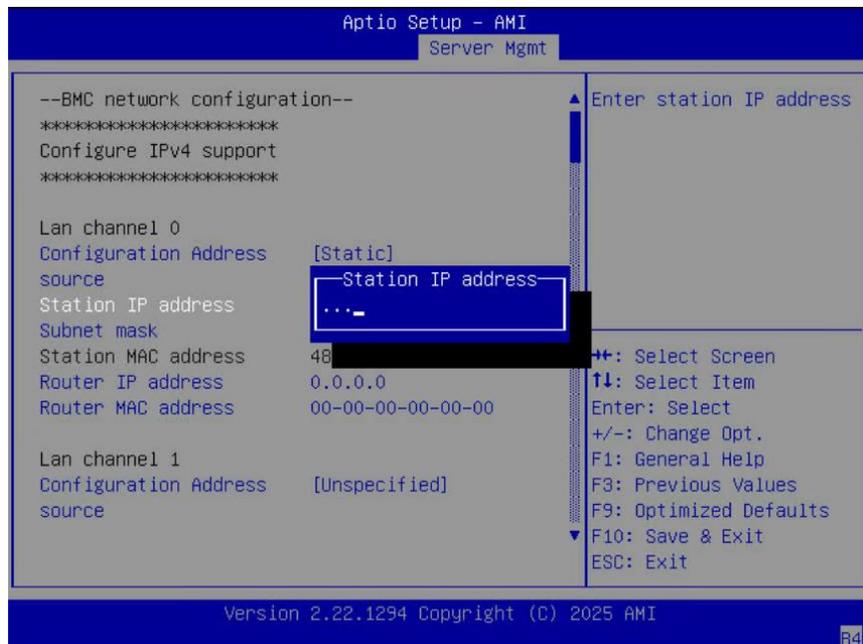


Figure 45. BIOS – BMC Static IP Configuration

```
System Information
AS400-2A1 System BIOS Version:0.62.00 Date:11/28/2025
B/P CPLD Version:0.53.00, M/B CPLD Version:0.59.00
BMC Version:0.63.00
Management Port 0 IP:10.255.114.75
Management Port 1 IP:0.0.0.0
CPU Info:AMD EPYC 9575F 64-Core Processor 5000MHz
Processor Family:AMD Zen Processor Family Model:02h Stepping:C1 Package:SP5
Processors:2 Dies:2 Cores:64 Threads:128
Memory Info: Memory Size:1024GB Memory Speed:4400MHz

-----
System Boot Status
0x4F : DXE IPL Start
0x60 : DXE Core Started.
0x63 : CPU DXE Initialization.
0x68 : PCI HB Initialization.
0x69 : NB DXE Initialization.
0x6A : NB DXE SMM Initialization.
0x70 : SB DXE Initialization.
0x79 : CSM Driver Entry point
0x90 : BDS Started.
0x91 : Connecting Drivers.

0091
```

Figure 46. Early POST - System Information

Note:

The Management IP (BMC IP) will be displayed on the system information screen during the POST process.
The Management port 0 IP comes from the dedicated LAN in BMC front panel.
The Management port 1 IP comes from the NVIDIA BF3 LAN0 through NC-SI interface.

Note:

The AS400-2A1 series doesn't support the NC-SI interface in ACPI S5. As a result, users can NOT upgrade BIOS by BMC WebUI or Redfish with NVIDIA BF3 LAN0 through the NC-SI interface.

8.2.5 Hot Keys

POST Stage

Table 35. POST Stage Hot Keys

F1	Skip the Error Pause. (if an error pause happens)
F2	Enter the BIOS Setup Menu. (if an error pause happens)
Del	Enter the BIOS Setup Menu
F10	Enter the Boot Menu
F12	Force Network Boot

Note:

Hot keys work in the remote target, e.g. iKVM and console redirection.

BIOS Menu

Table 36. BIOS Menu Hot Keys

F1	General Help
F3	Previous Values
F9	Optimized Default
F10	Save & Exit
ESC	Exit

8.3 AC Loss Function

BIOS and BMC should be synchronized in handling the AC power loss and the subsequent actions.

Table 37. AC Power Policy

AC Power Loss Condition	Last System Status	Next Time A/C Back
Power Off	System Off	System Keep Off
Power Off	System On	System Keep Off
Power On	System Off	System Keep On
Power On	System On	System Keep On
Last State	System Off	System Keep Off
Last State	System On	System Keep On

Note:

The power status is controlled by BMC; the CPU after G3 register is set to be powered off.

Chapter 9 Firmware Update

This chapter provides firmware update information (including BMC, BIOS, and CPLD) using the BMC WebUI or Redfish.

9.1 Using the BMC WebUI

Note:

Please be aware that all screenshots provided within this document are for reference only. While they offer a general idea of the interface, the actual web display you encounter may differ.

9.1.1 Logging in the BMC WebUI

Open a web browser and enter **https://10.255.114.151** (or the BMC IP you want to set up) to access the BMC WebUI.

BMC Default Account

An account with Administrator privileges is required to perform firmware updates using BMC out-of-band mechanisms like WebUI and Redfish. The default account of BMC WebUI is as below:

Username	admin
Password	admin

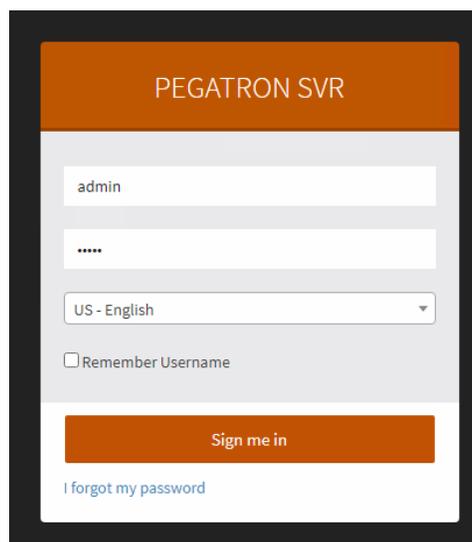
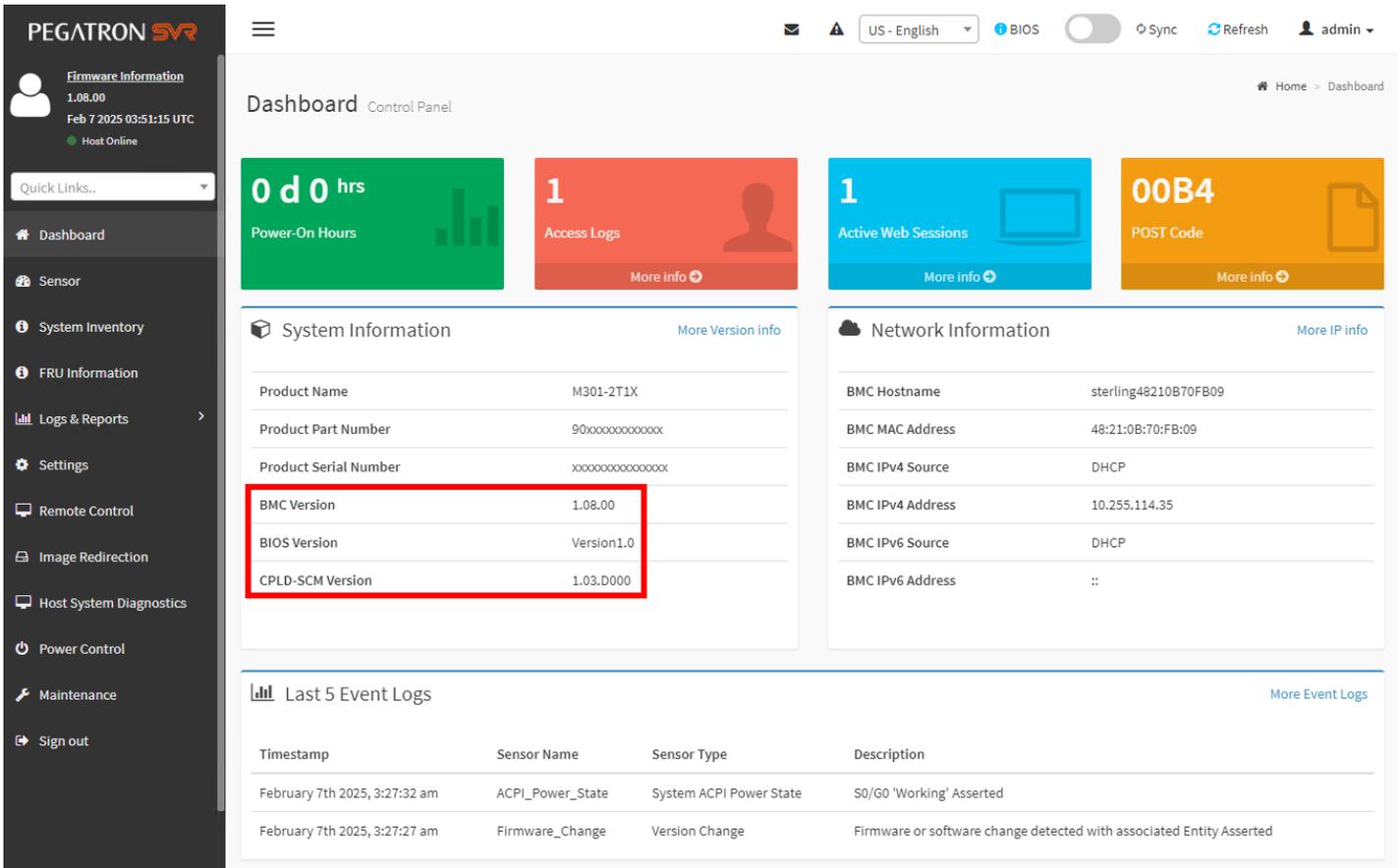


Figure 47. Logging in the BMC WebUI

9.1.2 Checking the Current Firmware Version

Once logging in, the Dashboard page will display the current firmware versions of BMC, BIOS, and CPLD as indicated below:



The screenshot shows the BMC WebUI Dashboard. The left sidebar contains navigation options: Dashboard, Sensor, System Inventory, FRU Information, Logs & Reports, Settings, Remote Control, Image Redirection, Host System Diagnostics, Power Control, Maintenance, and Sign out. The main content area is titled 'Dashboard Control Panel' and includes several widgets:

- Power-On Hours:** 0 d 0 hrs
- Access Logs:** 1
- Active Web Sessions:** 1
- POST Code:** 00B4
- System Information:** A table listing product details and firmware versions.
- Network Information:** A table listing network configuration details.
- Last 5 Event Logs:** A table showing recent system events.

The **System Information** table is highlighted with a red box, showing the following data:

Field	Value
Product Name	M301-2T1X
Product Part Number	90xxxxxxxxxxxx
Product Serial Number	xxxxxxxxxxxxxxxx
BMC Version	1.08.00
BIOS Version	Version1.0
CPLD-SCM Version	1.03.D000

Figure 48. BMC WebUI Dashboard Page

9.1.3 BMC Firmware Update

The Firmware Update page enables the user to perform all the Firmware Update operations for BMC, BIOS, or CPLD. Follow the instructions of the update wizard to work through the process of firmware update. The BMC will take about 2 minutes to reboot. The WebUI will not work while the BMC is rebooting. Refresh the webpage after the BMC has rebooted to access the WebUI as normal. The option to Preserve All Previous Configurations is available for BMC update. Check the checkbox to enable it if you wish to preserve configured settings through the update.

Note:

After entering the update mode widget, the other web pages and services of the BMC will not work. All open widgets will be closed automatically. If the Update process is cancelled in the middle of the wizard, the device will be reset.

Follow the instructions below to update firmware:

1. Click **Maintenance** on the sidebar and then click the **Firmware Update** box.

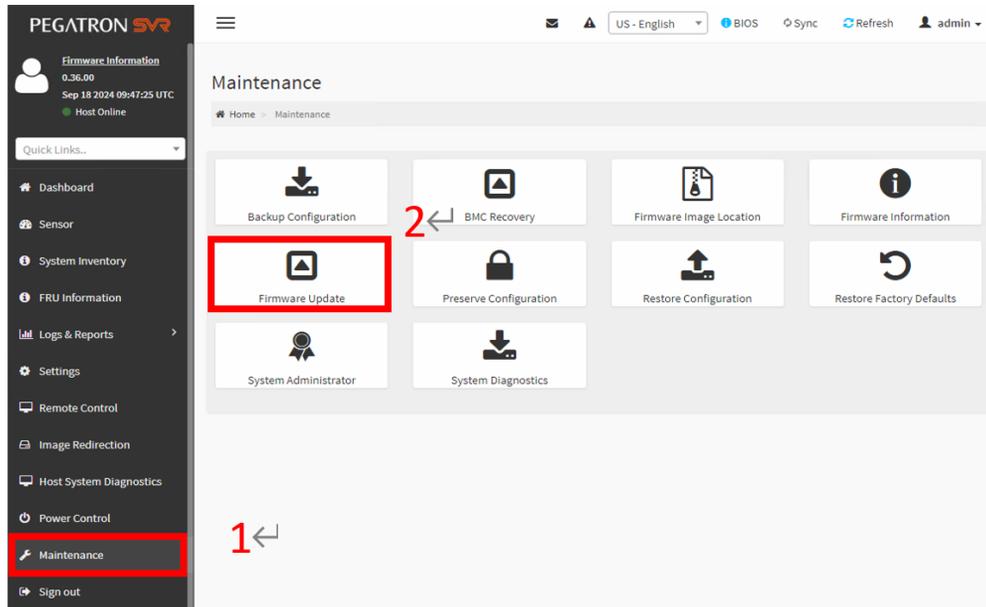


Figure 49. BCM Firmware Update – 1

2. Click the browse icon to select the new firmware image you want to use to update. (BMC uses an .ima file. **bmc_0.36.00.ima** is used as an example here.)

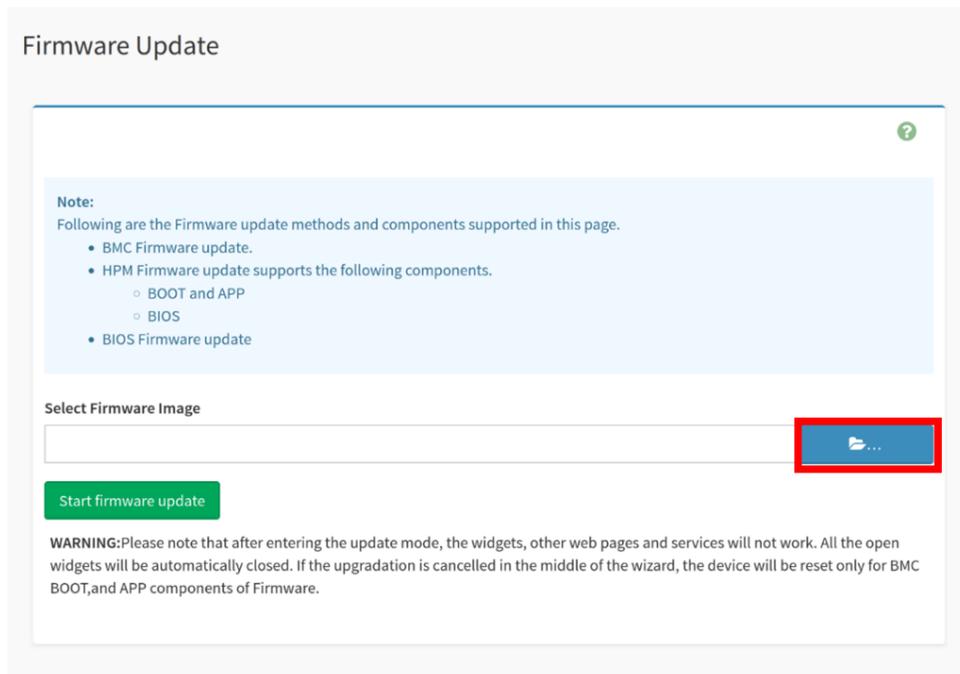


Figure 50. BMC Firmware Update - 2

3. Click **Start firmware update** to load firmware update information.

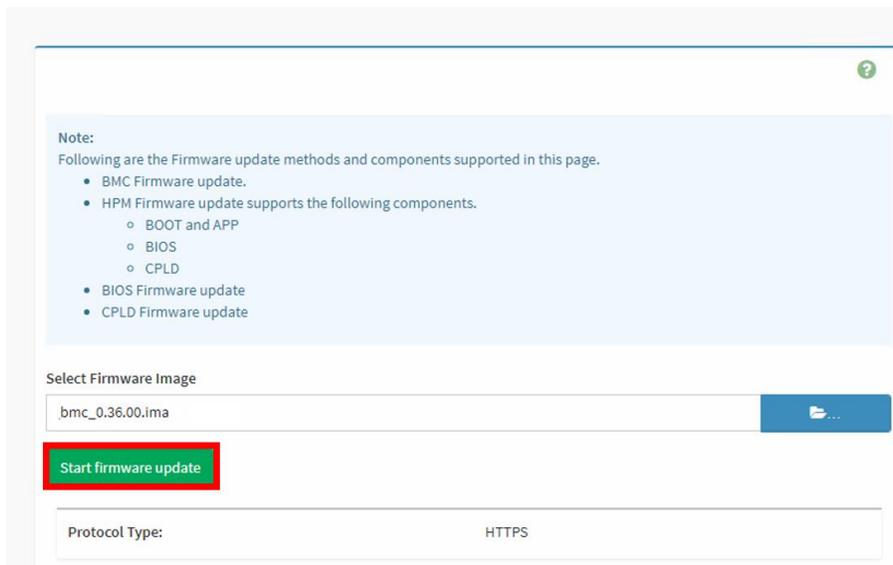


Figure 51. BMC Firmware Update - 3

4. Check **Preserve all Configuration** if you want to preserve all previous configurations and click **Edit Preserve Configuration** if you want to modify the Preserve status settings.

Note:

We recommend **NOT** preserving the previous configuration, since there might be some new updates in those regards. This wizard takes you through the process of AMI based firmware upgradation. The protocol information to be used for firmware image transfer during this update is as follows. All configuration items will be preserved/overwrite as default during the restore configuration operation.

Preserve all Configuration. This will preserve all the configuration settings during the firmware update - irrespective of the individual items marked as preserve/overwrite in the table below.

All configuration items below will be preserved as default during the restore configuration operation. Click "Edit Preserve Configuration" to modify the Preserve status settings.

[Edit Preserve Configuration](#)

S.No	Preserve Configuration Item	Preserve Status
1	SDR	Overwrite
2	FRU	Overwrite
3	SEL	Overwrite
4	IPMI	Overwrite
5	NETWORK	Overwrite
6	NTP	Overwrite
7	SNMP	Overwrite
8	SSH	Overwrite
9	KVM	Overwrite
10	AUTHENTICATION	Overwrite
11	SYSLOG	Overwrite
12	WEB	Overwrite
13	REDFISH	Overwrite

Figure 52. BMC Firmware Update - 4

- Click **Proceed to Flash** to start firmware update.

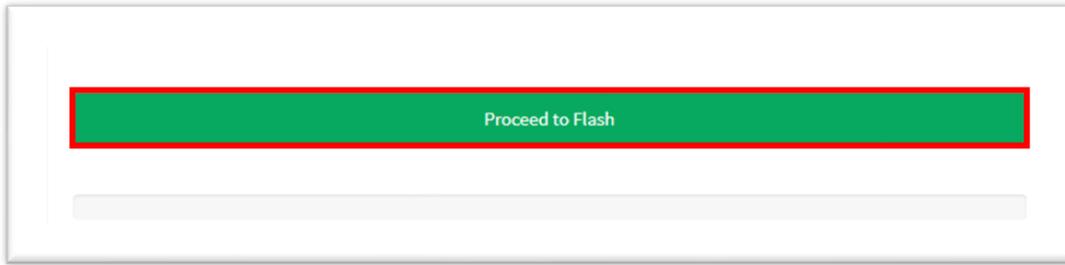


Figure 53. BMC Firmware Update - 5

- Click **OK** on the confirmation window that appears to start uploading the firmware file.

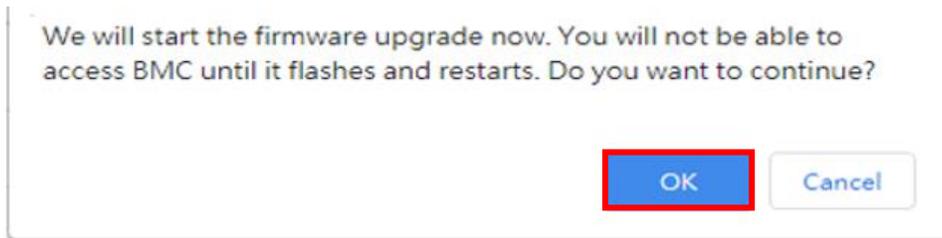


Figure 54. BMC Firmware Update - 6

- The firmware loading will take about one minute (depending on the networking speed). When the loading bar is half full and the text says "Uploading 100%," click **Flash to Proceed** to continue.

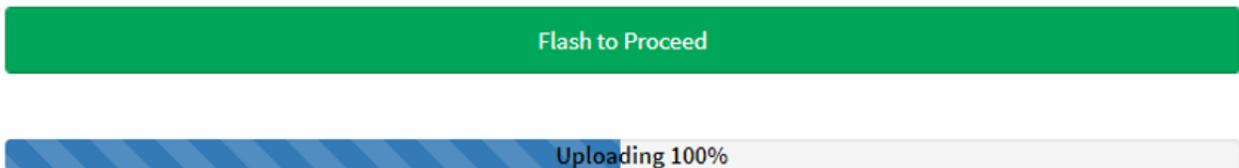


Figure 55. BMC Firmware Update - 7

- When the confirmation window appears, click **OK** to proceed. The update will take 6-7 minutes. Make sure the update process is not interrupted.

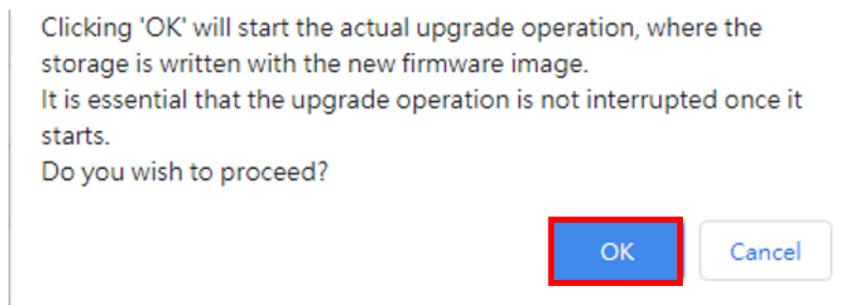


Figure 56. BMC Firmware Update - 8

9. After the BMC firmware is updated, the system will take about 180 seconds to restart. No functions will take effect until the BMC is ready. The following pop up will show up, prompting you to refresh the web page after a few minutes.

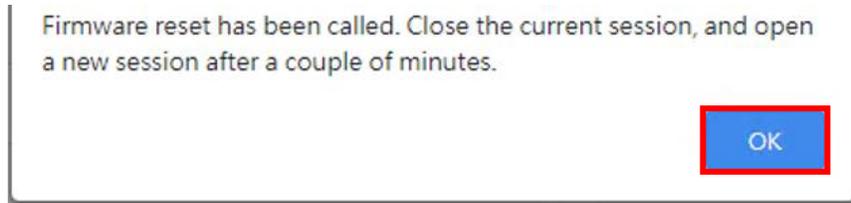


Figure 57. BMC Firmware Update - 9

9.1.4 BIOS Firmware Update

Note:

When users upgrade BIOS or CPLD via the BMC WebUI or redfish, the system should be on ACPI S5 to avoid any unexpected issues.

Follow the instructions below to update BIOS firmware using the WebUI:

1. Click **Maintenance** on the sidebar and then click the **Firmware Update** box.

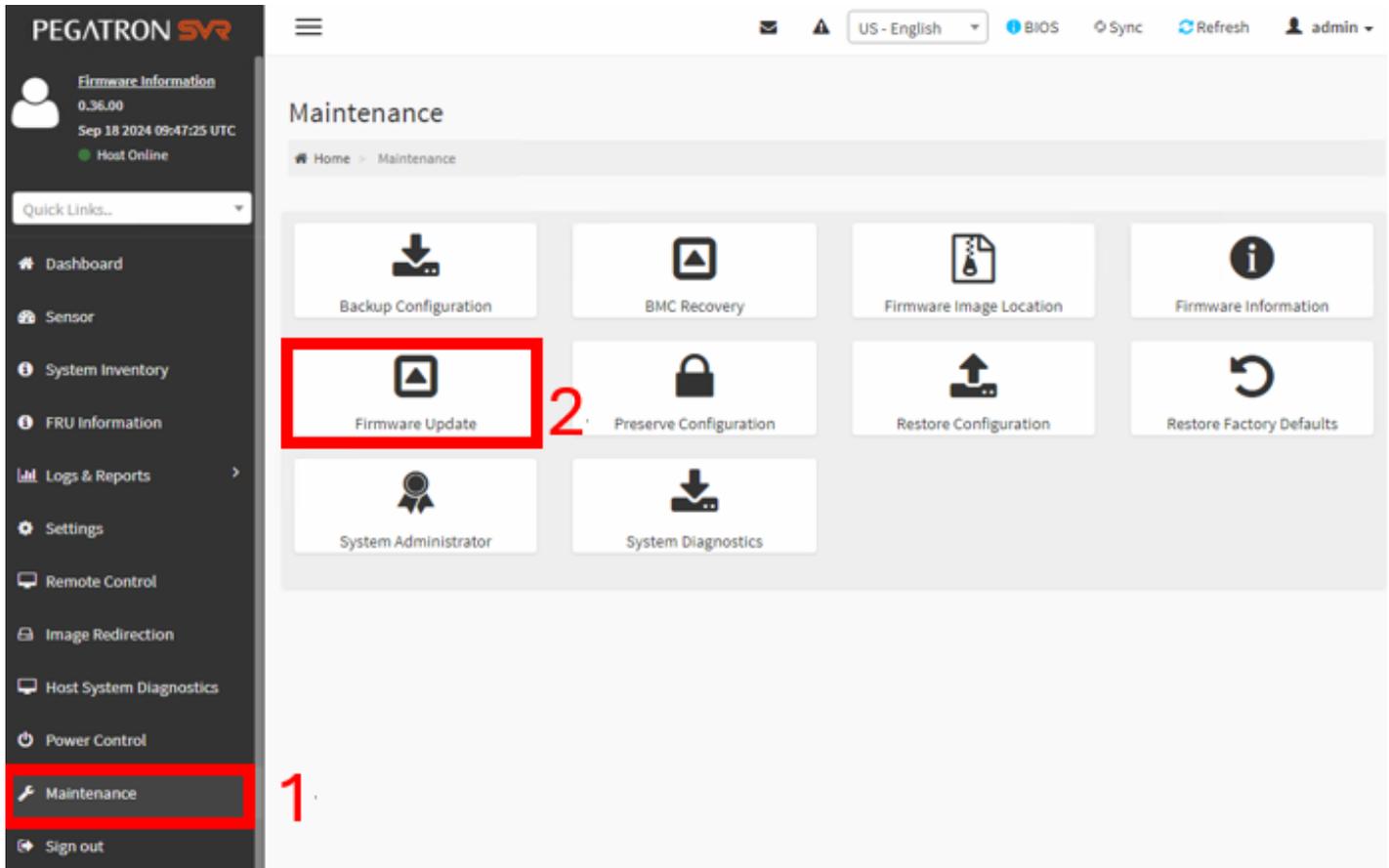


Figure 58. BIOS Firmware Update

2. Click the browse icon to select the BIOS firmware image you want to use to update BIOS. (BIOS uses a .bin file. **BIOS02700.bin** is used as an example here.)

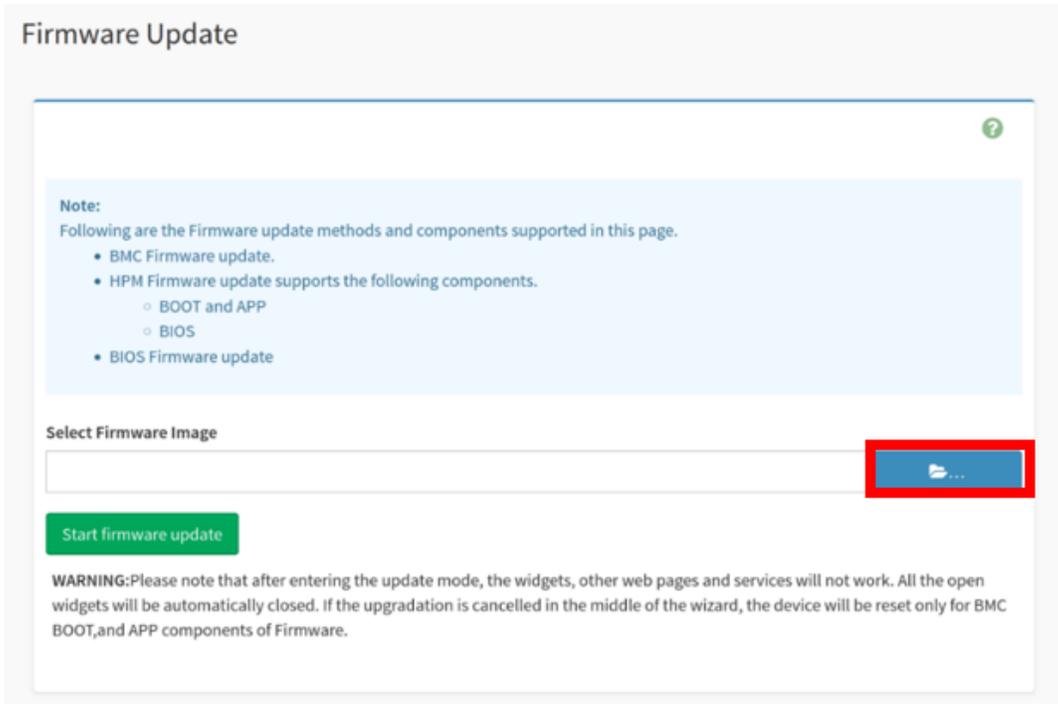


Figure 59. Browse to select the BIOS Firmware

3. Click **Start firmware update** to load the firmware update information.

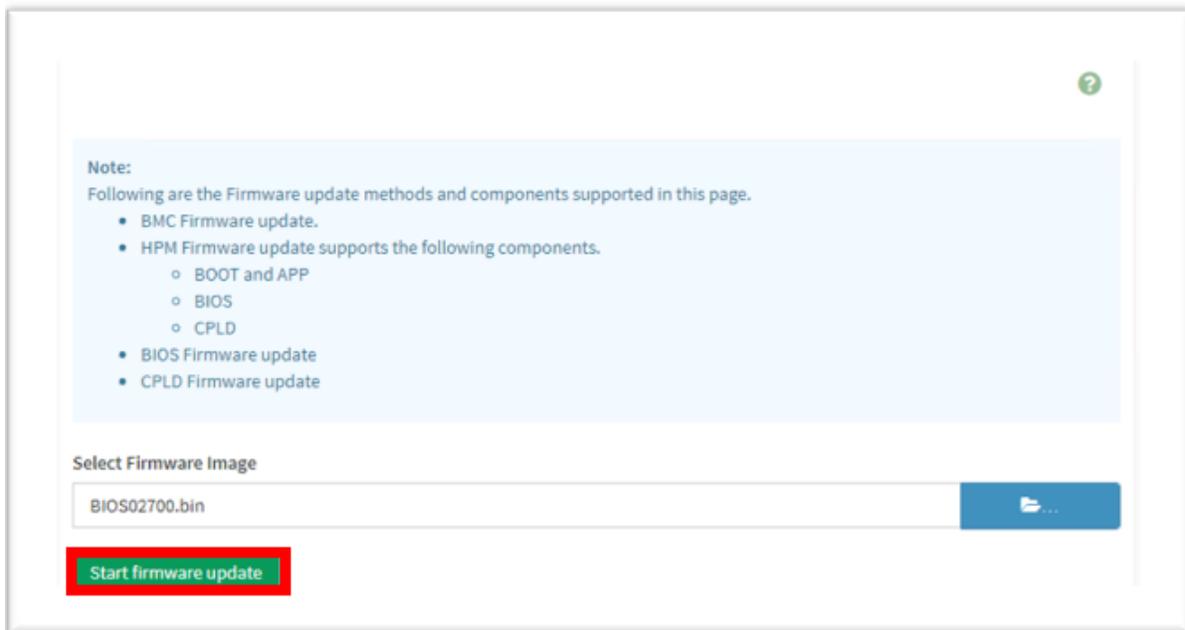


Figure 60. Start BIOS firmware update.

- Click **Proceed** to upload image

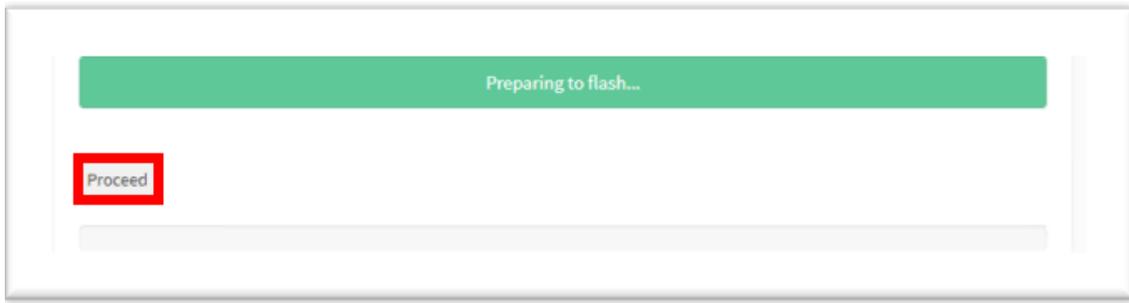


Figure 61. Proceed BIOS firmware update

- Click **OK** on the confirmation window that appears to proceed.

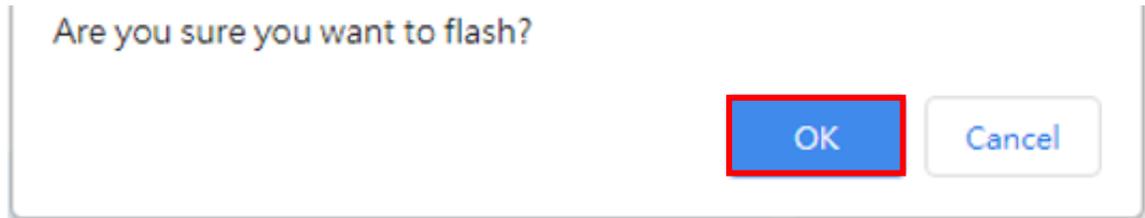


Figure 62. Are you sure you want to flash the BIOS firmware?

- Click **Proceed to flash image** to start firmware update. The update will take 1-2 minutes.

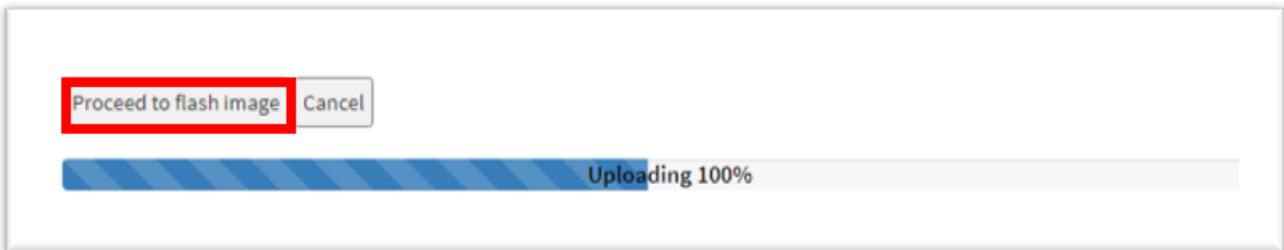


Figure 63. Proceed to flash BIOS image.

- After updating the BIOS, the system will remain powered off and needs to be turned on manually.

Note:

After updating the BIOS, the new version of information will not immediately be reflected in the BMC. The updated version will only be displayed after the system syncs the data back to the BMC. Please reboot the system and complete the POST process so that BMC can obtain updated BIOS information.

9.1.5 CPLD Firmware Update

Note:

When users upgrade BIOS or CPLD via the BMC WebUI or redfish, the system should be on ACPI S5 to avoid any unexpected issues.

Follow the instructions below to update BIOS firmware using the WebUI:

1. Click **Maintenance** on the sidebar and then click the **Firmware Update** box.

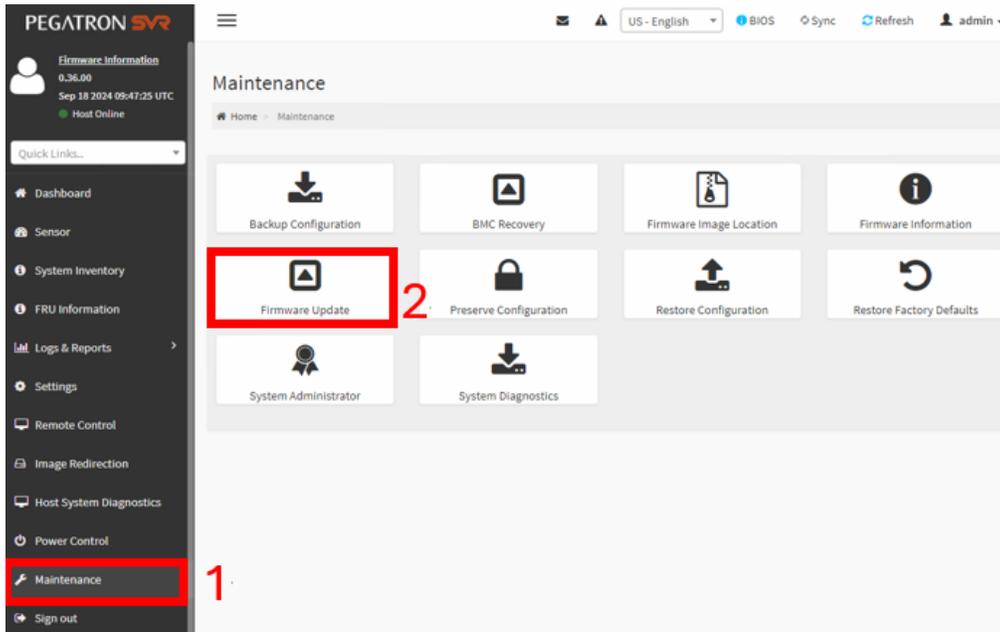


Figure 64. CPLD Firmware Update

2. Click **Browse** to select firmware images you want to use to update CPLD. There are three types of CPLD: HPM, SCM and HSBP (High Speed BackPlane). Some machines don't have HSBP or don't support HSBP CPLD firmware update by BMC WebUI. All CPLD uses < signed_cpld.jed> or < signed_cpld.hpm> files to update firmware.

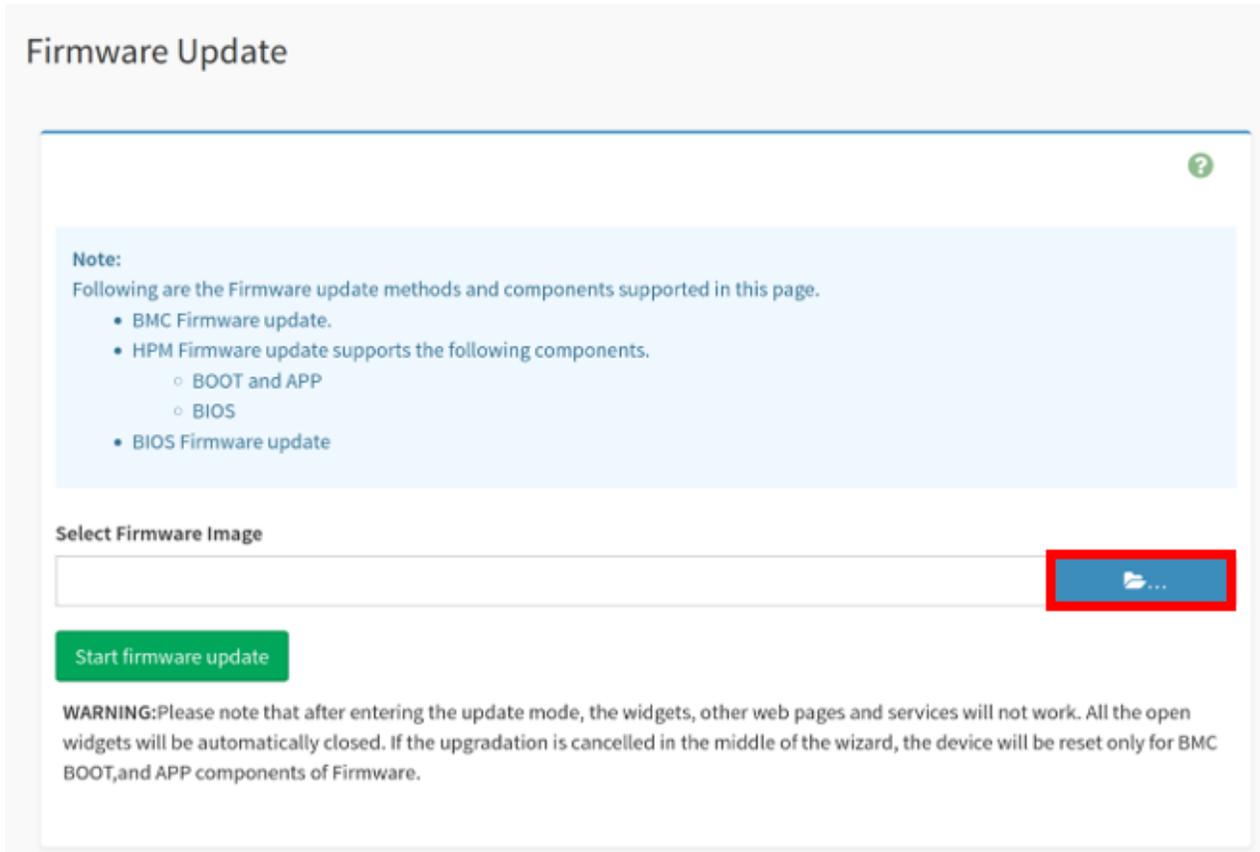
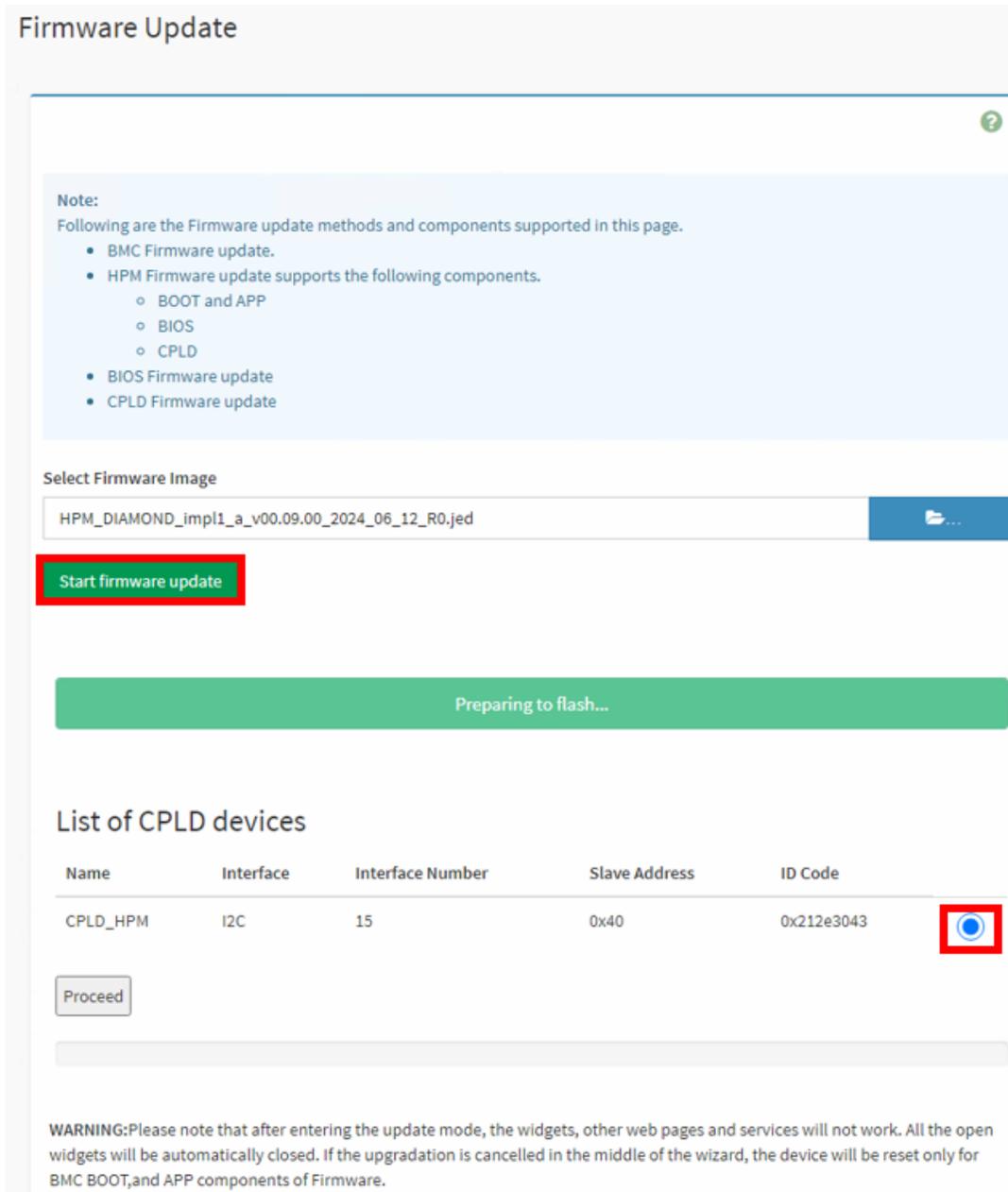


Figure 65. CPLD Firmware Widget

3. Click **Start firmware update** to load the Firmware Update information.
In this example, the file we are using is
“HPM_DAIMOND_impl1_a_v00.09.00_2024_06_12_R0.jed”.



Firmware Update

Note:
Following are the Firmware update methods and components supported in this page.

- BMC Firmware update.
- HPM Firmware update supports the following components.
 - BOOT and APP
 - BIOS
 - CPLD
- BIOS Firmware update
- CPLD Firmware update

Select Firmware Image

HPM_DIAMOND_impl1_a_v00.09.00_2024_06_12_R0.jed

Start firmware update

Preparing to flash...

List of CPLD devices

Name	Interface	Interface Number	Slave Address	ID Code	
CPLD_HPM	I2C	15	0x40	0x212e3043	

Proceed

WARNING: Please note that after entering the update mode, the widgets, other web pages and services will not work. All the open widgets will be automatically closed. If the upgradation is cancelled in the middle of the wizard, the device will be reset only for BMC BOOT, and APP components of Firmware.

Figure 66. Start CPLD Firmware Update

In this second example, the file we are using is “SCM_DAIMOND_impl1_a_v00.08.01_CPLD_SYS_ER_LED.jed”.

Select Firmware Image

SCM_DIAMOND_impl1_a_v00.08.01_CPLD_SYS_ER_LED.jed

Start firmware update

Preparing to flash...

Update All

List of Components

#	Component Name	Existing Version	Uploaded Version	Upgrade
1	CPLD_SCM	0.0.0	0.8.1	<input checked="" type="checkbox"/>

List of CPLD devices

Name	Interface	Interface Number	Slave Address	ID Code	Firmware Version	
CPLD_SCM	I2C	0xf	0x44	0x212e3043	0x0	<input checked="" type="radio"/>

Proceed

WARNING:Please note that after entering the update mode, the widgets, other web pages and services will not work. All the open widgets will be automatically closed. If the upgradation is cancelled in the middle of the wizard, the device will be reset only for BMC BOOT,and APP components of Firmware.

Figure 67. Start CPLD Firmware Update

4. Click **Proceed** to start firmware update

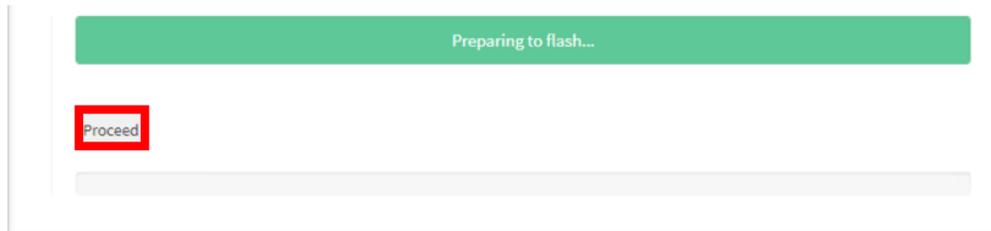


Figure 68. Proceed with CPLD Firmware update

5. In the confirmation window that appears, click **OK** to proceed.

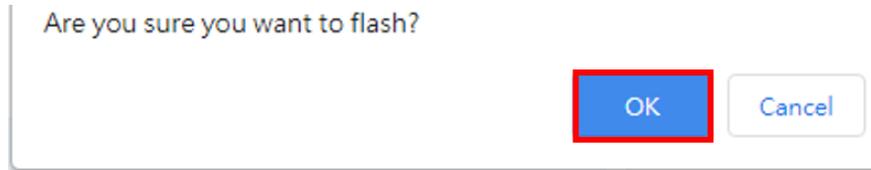


Figure 69. Are you sure you want to flash CPLD Firmware?

6. The update will take about 5 to 6 minutes. When the update is complete, the following notice window will appear. Click **OK** to complete the procedure.

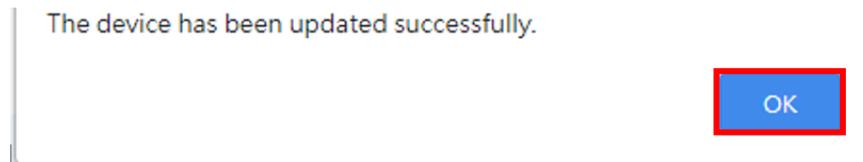


Figure 70. CPLD Firmware Update Successfully

9.2 Using Redfish

The Redfish Scalable Platforms Management API ("Redfish") is a specification that uses RESTful interface semantics to access data defined in model format to perform out-of-band systems management. It is suitable for a wide range of servers, from stand-alone servers to rack mount and bladed environments but scales equally well for large scale cloud environments.

9.2.1 Preparation

Install CPLD, which is a computer software project providing a library (libcurl) and command-line tool (curl) for transferring data using various network protocols. The following sections will use cURL to send a Redfish request to BMC.

Use WebUI to check the firmware versions your system is using. Refer to Chapter 9.1.2 "Current Firmware Version" for guidance. **(Robin: no link)**

9.2.2 Multipart Push FW Update

The BMC provides a multipart push to update BMC firmware and other component with HPM image, .bin BIOS image format and .jed CPLD image format. In the following example, we use curl to send the Redfish Request, please follow the steps as given below.

Create a JSON file "parameters.json" with content like below.

```
{
  "Targets": [
    "/redfish/v1/UpdateService/FirmwareInventory/BMC"
  ]
}
```

Create a JSON file "oem_parameters.json" with content like below.

```
{
  "ImageType": "BMC"
}
```

(Optional) Using curl to send the request to power off the system if updating BIOS.

```
curl -k -u 'admin:admin' -X POST \
https://10.255.114.67/redfish/v1/Systems/Self/Actions/ComputerSystem.Reset \
-H 'Content-Type: application/json' -H 'If-match: *' \
-d '{"ResetType": "GracefulShutdown"}
```

Using curl to send the request to update firmware.

```
curl -k --http1.0 -u 'admin:admin' -X POST \  
https://10.255.114.67/redfish/v1/UpdateService/upload \  
-H 'Content-Type: multipart/form-data' \  
--form 'UpdateParameters=@"/tmp/parameters.json";type=application/json' \  
--form 'OemParameters=@"/tmp/oem_parameters.json";type=application/json' \  
--form 'UpdateFile=@"/tmp/bmc.ima";type=application/octet-stream'
```

The response should be like the screenshot below.

```
{  
  "@odata.id": "/redfish/v1/TaskService/Tasks/1",  
  "@odata.type": "#Task.v1_4_2.Task",  
  "Description": "Task for Update Service Task",  
  "Id": "1",  
  "Messages": [  
    {  
      "@odata.type": "#Message.v1_0_8.Message",  
      "Message": "The action UpdateService.MultipartPush was submitted to do firmware update.",  
      "MessageArgs": [  
        "UpdateService.MultipartPush"  
      ],  
      "MessageId": "UpdateService.1.0.StartFirmwareUpdate",  
      "Resolution": "None",  
      "Severity": "OK"  
    }  
  ],  
  "Name": "Update Service Task",  
  "StartTime": "2024-04-18T22:46:02+04:00",  
  "TaskMonitor": "/redfish/v1/TaskService/TaskMonitors/1",  
  "TaskState": "New",  
  "TaskStatus": "OK"  
}
```

Figure 71. Firmware Updates Successfully

9.2.3 Parameters of Multipart Push

The description of the parameters is given on the table below.

Part Name	Description
UpdateFile	Image binary for update
UpdateParameters	DMTF defined standard parameters (such as Targets) in JSON format
OemParameters	AMI OEM parameters (such as ImageType) in JSON format

The details of UpdateParameters and OemParameters are given in the table below.

Part	Parameter Name	Type	Allowed Value	Description
Update Parameters	Targets	Array of URI	/redfish/v1 /UpdateService /FirmwareInventory /BMC redfish/v1 /UpdateService /FirmwareInventory /BIOS redfish/v1 /UpdateService /FirmwareInventory /CPLD-{{cpld-instance}}	Indicates where to apply the update image. These targets should correspond to Firmware Inventory instances. If this property is not present or contains no targets, Redfish shall apply the software image to all applicable targets, as determined by the Redfish.
Oem Parameters	ImageType	String	BMC BIOS CPLD HPM	Indicate the format of image

For the {{cpld-instance}}, you can use redfish to get to redfish/v1/UpdateService/FirmwareInventory to see what instances exists. An alternative method would be to check your BMC firmware specifications for the firmware inventory.

Image Type	Description
BMC	Indicates uploaded file is a BMC image.
BIOS	Indicates uploaded file is a BIOS image.
CPLD	Indicates uploaded file is a CPLD image.
HPM	Indicates uploaded file is a HPM format.

The Targets of Update Parameters are mentioned in the following table.

If Targets property is not present or contains no targets, Redfish shall apply the software image to all applicable targets, as determined by the Redfish.

Targets	Description
/redfish/v1/UpdateService/FirmwareInventory/BMC	Indicates to update BMC firmware.
/redfish/v1/UpdateService/FirmwareInventory/BIOS	Indicates to update BIOS component.
/redfish/v1/UpdateService/FirmwareInventory/CPLD	Indicates to update CPLD component.

Note:

After updating the BIOS, the new version of information will not immediately be reflected in the BMC. The updated version will only be displayed after the system syncs the data back to the BMC. Please reboot the system and complete the POST process so that BMC can obtain updated BIOS information.

Appendix A: Hardware Information should be noted

1. For CMOS battery removal or installation, please follow the instructions in the **CMOS Battery** section under the hardware maintenance chapter.
2. For CMOS-clear, AMD recommends users to clear CMOS while the system is AC off (in G3 status).
If the user clears the CMOS of the system in S5, the system can NOT be powered-on unless the system is AC off then AC on.
3. The AS400-2A1 series doesn't support NC-SI connectivity with the NVIDIA B3220 or other PCIe networking cards in ACPI S5 (soft-off) power state. As a result, you **MUST** use a **1GbE RJ-45 LAN cable** to connect to the BMC's dedicated front I/O LAN port when upgrading the **BIOS** via the **BMC WebUI** or **Redfish** in ACPI S5 (soft-off) power state.
4. The PCIe signals for M.2 SSD are sent from CPU0 P4 controller and the system supports M.2 SSD up to **PCIe Gen3 x2** bandwidth.
By default, only the 1st M.2 PCIe root port is enabled for NVIDIA NVQUAL item #24 and #26 testing. Users who do not require NVQUAL certification can **enable the 2nd M.2 root port via the BIOS settings**.
5. There will be Bus Correctable errors and unknown #0xa3/#0xa4 events when hot plugging an E1.S SSD out of the system This is a known issue for Broadcom/PEX89144 PCIe switch.
6. It requires an active official NVIDIA GPU driver for the BMC to accurately report NVIDIA GPU temperatures. In the absence of an official driver, a temperature-dependent margin of error is introduced; this discrepancy may exceed 3°C as operating temperatures rise. As a result, GPU sensor data may be inaccurate during system boot-up state, power-off state, or within operating systems lacking the official driver (e.g., when running NVIDIA NVQUAL).
7. Running NVIDIA NVQUAL replaces the official NVIDIA GPU driver with the DOCA driver. As a result, GPU temperature readings reported via the BMC may become inaccurate.
8. The system supports 4 pcs 8080 fans **with only one rotor fan fail support in ACPI S0**.
9. The USB 3.0 port at the rear side of the system **doesn't support USB3.0 Hub**.
10. The system supports **CRPS 3+1 configuration with ONLY AC 220V input**. Platform management will set the system power configuration to 3+1 (Redundant Power) if it detects 4 pcs functional power supplies. In a redundant power configuration, if one power supply fails, the backup power supply will automatically engage and provide the necessary power to maintain optimal system operation. With 1 pcs power supply failure, the BMC will generate several events that are registered to the system event log (SEL) and change the system power configuration to 3 + 0 (non-

redundant) until the failed power supply is replaced. In addition, the System Status LED on the front side of the system will change to solid amber, denoting a degraded but operational system state.

Platform management will set the system power configuration to **CRPS 3+0 configuration** (non-Redundant power configuration) **with ONLY AC 220V input** when it detects that the system has only 3 pcs power supply installed. With a single functional power supply, the system has no power redundancy and the total available power to the system is limited to the maximum power capacity of the power supply. Should the system power draw exceed the power limits of the power supply, server management will enable throttling which limits I/O performance to system processors or enable power brake which limits performance to of GPU.

Appendix B: Software Information should be noted

1. The system can't be installed with RHEL9.4 OS (No matter what Kernal it is) via PXE (Preboot eXecution Environment) with NV BlueField-3 B3220 PCIe DPU Card, but it's PASS for RHEL 9.2 (5.14.0-284.11.1.el9_2) and RHEL 9.6 (5.14.0-570.12.1.el9_6).
It's a known issue listed in <https://access.redhat.com/solutions/7116976> (Should login with developer for the detailed information)
2. To compliant with the mini-DP to DP/HDMI/D-sub dongle, the mini-DisplayPort does not support 2D mode resolution of 1280 x 720 and 1280 x 960
3. It is expected that the system will automatically reboot once when first booting to the POST screen after a BIOS update via the BMC WebUI or UEFI Shield. This behavior will not recur afterward.
4. When users upgrade BIOS or CPLD via the BMC WebUI or redfish, the system should be on ACPI S5 to avoid any unexpected issues.
5. After BIOS upgrade successfully to new version, please power on the system then make sure the system runs BIOS post code completely (the system finally should be in uEFI shield or OS / BIOS setup menu), then users can reload BMC WebUI to get correct BIOS firmware information.
6. The system supports two GPU options, including NVIDIA® H200 NVL / RTX PRO 600. If users want to get any information about NVIDIA GPU card (Ex: Temperature Sensor data), please load driver and enable driver persistence mode first, for example, in the Ubuntu GUI mode. Below is the information about the NVIDIA driver Persistence mode, and the command to enable the feature is "`# nvidia-smi -pm ENABLED`"
<https://docs.nvidia.com/deploy/driver-persistence/index.html>
7. It requires an active system driver for BMC to accurately report NVIDIA GPU temperature sensor data. Absence of a driver introduces a temperature-dependent margin of error, which may exceed 3°C as operating temperatures increase.
8. The memory in NVIDIA H200 NVL GPU card is HBM3e and the memory in NVIDIA RTX PRO 6000 GPU card is GDDR7. Users can obtain memory temperature information of H200 NVL or RTX PRO 6000 by BMC WebUI / SDR with NVIDIA SMBus Post-Box interface (SMBPBI) for GPUs protocol. However, it requires an active system driver for BMC to accurately report NVIDIA GPU temperature sensor data.
9. It is recommended to configure the BMC dedicated IP address using dynamic allocation (the default BIOS setting) with Ethernet DHCP supported) as the BMC will not provide any error message in case of an IP address conflict.

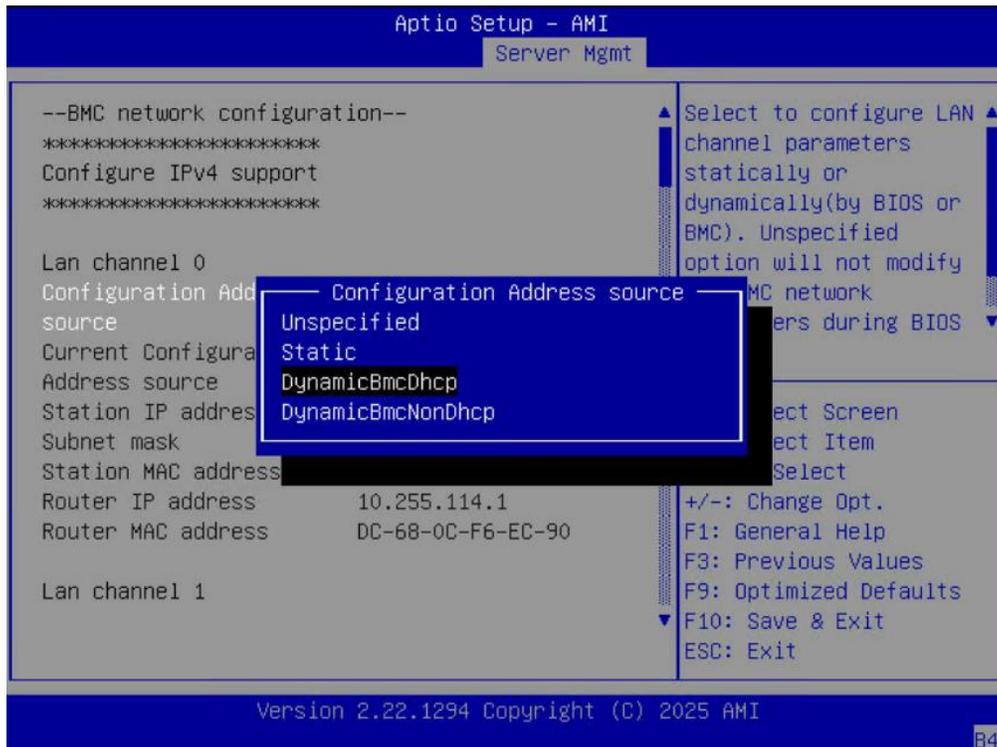


Figure 72. BIOS - BMC IP Configuration

10. The PCIe signals for M.2 SSD are sent from CPU0 P4 controller and the system supports M.2 SSD up to **PCIe Gen3 x2** bandwidth.

By default, only the 1st M.2 PCIe root port is enabled for NVIDIA NVQUAL item #24 and #26 testing. Users who do not require NVQUAL certification can **enable the 2nd M.2 root port via the BIOS settings.**

Appendix C: HPM Board Connector Pin Definitions

Function	Header Reference	Pin Description
For Fan	J_VTFAN1, J_RAFAN1	Pin1: P3V3_AUX Pin2: GND Pin3: FAN SMBus Clock Pin4: FAN SMBus Data Pin5: FAN SMBus Alert Pin6: NC Pin7: NC Pin8: NC
For Rear I/O board	J_IOBD	Pin1: P5V_AUX Pin2: P3V3_AUX Pin3: GND Pin4: FP_UID_BTN_L Pin5: CPLD_UID_LED Pin6: CPLD_SYS_ER_LED Pin7: CPLD_PWR_BTN_O_L Pin8: CPLD_PWR_BTN_G_L Pin9: FP_PWR_BTN_L Pin10: FP_RST_BTN_L Pin11: SMB_IOBD_SCL Pin12: SMB_IOBD_SDA
Main Power For HPM board	J_MBPWR1, J_MBPWR2, J_MBPWR3	Pin1: GND Pin2: GND Pin3: GND Pin4: GND Pin5: P12V Pin6: P12V Pin7: P12V Pin8: P12V
Standby Power For HPM board	J_MBSTBY	Pin1: GND Pin2: P12V_STBY
Standby Power For HPM board	J_BF3PWR	Pin1: GND Pin2: GND Pin3: GND Pin4: P12V_AUX Pin5: P12V_AUX

Function	Header Reference	Pin Description	
		Pin6: P3V3	
Main Power For NIC	J_NICPWR	Pin1: GND Pin2: GND Pin3: GND Pin4: GND Pin5: P12V Pin6: P12V Pin7: P3V3 Pin8: P3V3	
Standby Power For front I/O board	J_IOPWR1	Pin1: GND Pin2: P12V_AUX	
For front I/O board	J_FARIO1	A Side Pin1: GND Pin2: SGMII_HPM_RX_DP Pin3: SGMII_HPM_RX_DN Pin4: GND Pin5: SCM_DP_TXD0_DP Pin6: SCM_DP_TXD0_DN Pin7: GND Pin8: FIO_PWR_BTN_N Pin9: FIO_PWR_LED_N Pin10: FIO_RST_BTN_N Pin11: FIO_ID_BTN_N Pin12: FIO_ID_LED_N Pin13: GND Pin14: NC Pin15: NC Pin16: GND Pin17: NC Pin18: NC Pin19: GND Pin20: NC Pin21: NC Pin22: GND Pin23: NC Pin24: NC Pin25: GND Pin26: I2C_FIO_SCL Pin27: I2C_FIO_SDA Pin28: HPM_PRSNT_N Pin29: NC Pin30: NC	B side Pin1: GND Pin2: SGMII_TX_DP Pin3: SGMII_TX_DN Pin4: GND Pin5: SCM_DP_TXD1_DP Pin6: SCM_DP_TXD1_DN Pin7: GND Pin8: UART_BMC_TX Pin9: UART_BMC_RX Pin10: NC Pin11: UART_CPU_TX Pin12: UART_CPU_RX Pin13: GND Pin14: NC Pin15: NC Pin16: GND Pin17: NC Pin18: NC Pin19: GND Pin20: NC Pin21: FIO_PRSNT_N Pin22: GND Pin23: FIO_DP_LD_SW_EN Pin24: FIO_DP_HPDP Pin25: GND Pin26: FIO_USB_OC_N Pin27: FIO_USB_PWR_EN Pin28: FIO_PHY_RST_N Pin29: FIO_PHY_MDC Pin30: FIO_PHY_MDIO

Function	Header Reference	Pin Description	
		Pin31: GND Pin32: BMC_DP_AUX_DP Pin33: BMC_DP_AUX_DN Pin34: GND Pin35: FIO_USB3_RX_DP Pin36: FIO_USB3_RX_DN Pin37: GND	Pin31: GND Pin32: FIO_USB2_DP Pin33: FIO_USB2_DN Pin34: GND Pin35: FIO_USB3_TX_DP Pin36: FIO_USB3_TX_DN Pin37: GND
For PDB board	J_PDB_A1, J_PDB_B1, J_PDB_C1	Pin1: PA_PSU0_PRSNT_R_N Pin2: PA_PSU1_PRSNT_R_N Pin3: PA_PSU2_PRSNT_R_N Pin4: PA_PSU3_PRSNT_R_N Pin5: PA_PSU0_PWR_OK_R Pin6: PA_PSU1_PWR_OK_R Pin7: PA_PSU2_PWR_OK_R Pin8: PA_PSU3_PWR_OK_R Pin9: PDB_A_PWR_ON_N Pin10: PDB_A_ALERT_N_R Pin11: PA_PSU01_AC_OK_R1 Pin12: I2C_BMC_HPM_IPMB_PDB_A_R_SDA Pin13: PDB_A_LOAD_SHARE Pin14: I2C_BMC_HPM_IPMB_PDB_A_R_SCL Pin15: NC Pin16: GND Pin17: PA_PSU23_AC_OK_R1 Pin18: PDB_A_P12V_SENSE_P Pin19: PDB_A_COLD_REDUNDANT Pin20: PDB_A_P12V_SENSE_N	
NC-SI For NVIDIA BF3 B3220	J_NCSI1	Pin1: GND Pin2: BF3_PKG_ID1 Pin3: NCSI_BF3_ISO_RXD0 Pin4: CLK_50M_NCSI_BF3 Pin5: NCSI_BF3_ISO_RXD1 Pin6: GND Pin7: NCSI_BF3_ISO_CRSDV Pin8: HPM_NCSI_RBT_ISO_N Pin9: GND Pin10: BF3_PKG_ID0 Pin11: NCSI_BF3_ISO_R_TXEN Pin12: GND Pin13: NCSI_BF3_ISO_R_TXD0 Pin14: COM_UART3_BMC_BF3_TX Pin15: NCSI_BF3_ISO_R_TXD1 Pin16: COM_UART3_BMC_BF3_RX Pin17: NCSI_PRESENCE_A_N Pin18: GND Pin19: NCSI_BF3_ISO_ARBOUT	

Function	Header Reference	Pin Description	
		Pin20: NCSI_BF3_SIO_ARBIN	
	J_NVHMC (Reserved)	<p>A Side</p> <p>Pin1: GND</p> <p>Pin2: P3E_CPU1_P4_RX_HMC_DP0</p> <p>Pin3: P3E_CPU1_P4_RX_HMC_DN0</p> <p>Pin4: GND</p> <p>Pin5: P3E_CPU1_P4_RX_HMC_DP1</p> <p>Pin6: P3E_CPU1_P4_RX_HMC_DN1</p> <p>Pin7: GND</p> <p>Pin8: HMC_MAIN_PWR_EN</p> <p>Pin9: HMC_STBY_PWR_EN</p> <p>Pin10: HMC_STBY_PWR_PGOOD</p> <p>Pin11: HPM_HMC_PCIE_PERST_R_N</p> <p>Pin12: FPGA_HMC_R_SNN</p> <p>Pin13: GND</p> <p>Pin14: CLK_100M_CPU1_P4_A_DP</p> <p>Pin15: CLK_100M_CPU1_P4_A_DN</p> <p>Pin16: GND</p> <p>Pin17: SMB_SCM_HMC_2_LVC3_SCL</p> <p>Pin18: SMB_SCM_HMC_2_LVC3_SDA</p> <p>Pin19: GND</p>	<p>B side</p> <p>Pin1: GND</p> <p>Pin2: P3E_CPU1_P4_TX_C_HMC_DP0</p> <p>Pin3: P3E_CPU1_P4_TX_C_HMC_DN0</p> <p>Pin4: GND</p> <p>Pin5: P3E_CPU1_P4_TX_C_HMC_DP1</p> <p>Pin6: P3E_CPU1_P4_TX_C_HMC_DN1</p> <p>Pin7: GND</p> <p>Pin8: HMC_GLOBAL_WP_N</p> <p>Pin9: HMC_EROT_NRESET_N</p> <p>Pin10: HMC_FATAL_ERROR_N</p> <p>Pin11: HMC_EROT_RECOV_N</p> <p>Pin12: HMC_SCM_I2C_ALERT_N</p> <p>Pin13: GND</p> <p>Pin14: SMB_SCM_HMC_1_LVC3_SCL</p> <p>Pin15: SMB_SCM_HMC_1_LVC3_SDA</p> <p>Pin16: GND</p> <p>Pin17: USB2_HUB_2517_0_P7_DP</p> <p>Pin18: USB2_HUB_2517_0_P7_DN</p> <p>Pin19: GND</p>
Main Power For backplane	J_BPM2PW	<p>Pin1: GND</p> <p>Pin2: GND</p> <p>Pin3: GND</p> <p>Pin4: GND</p> <p>Pin5: P12V</p> <p>Pin6: P12V</p> <p>Pin7: P3V3</p> <p>Pin8: P3V3</p>	
I2C for backplane	BP_I2C_1, BP_I2C_2, BP_I2C_3	<p>Pin1: P3V3_AUX</p> <p>Pin2: SMB_SCL</p> <p>Pin3: SMB_SDA</p> <p>Pin4: GND</p>	
Intruder	H_INTRUN	<p>Pin1: INTRUDER</p> <p>Pin2: GND</p>	

Function	Header Reference	Pin Description	
		Pin 1- Pin 2: Short <Chassis Closed> Pin 1- Pin 2: Open <Chassis Open >	
Clear CMOS	H_CLRRTC	Pin 1- Pin 2 : NORMAL - DEFAULT Pin 2- Pin 3 : CLEAR CMOS	
NVIDIA DC-SCi	NV_SCM1	<p>A Side</p> <p>PinOA1: GND PinOA2: NC PinOA3: NC PinOA4: GND PinOA5: SCM_DP_TXD0_DN PinOA6: SCM_DP_TXD0_DP PinOA7: GND PinOA8: SGMII_RTL8211_HPM_TX_C_DN PinOA9: SGMII_RTL8211_HPM_TX_C_DP PinOA10: GND PinOA11: SCM_DP_TXD1_DN PinOA12: SCM_DP_TXD1_DP PinOA13: GND PinOA14 : GND</p> <p>Pin1: P12V_AUX Pin2: P12V_AUX Pin3: P12V_AUX Pin4: P12V_AUX Pin5: GND Pin6: GND Pin7: GND Pin8: JTAG_SCM_TCK_LVC3 Pin9: JTAG_SCM_TDI_LVC3 Pin10: JTAG_SCM_TDO_LVC3 Pin11: JTAG_SCM_TMS_LVC3 Pin12: JTAG_SCM_TRST_LVC3 Pin13: SCM_HPM_STBY_RST_N Pin14: SCM_HPM_STBY_EN Pin15: I2C_BMC_HPM_FRU_SCL Pin16: I2C_BMC_HPM_FRU_SDA Pin17: SMB_SCM_I2C6_LVC3_SCL Pin18: SMB_SCM_I2C6_LVC3_SDA Pin19: GND Pin20: NC Pin21: NC Pin22: GND</p>	<p>B Side</p> <p>PinOB1: GND PinOB2: NC PinOB3: NC PinOB4: GND PinOB5: SCM_DP_AUX_DN PinOB6: SCM_DP_AUX_DP PinOB7: GND PinOB8: SGMII_HPM_RTL8211_RX_DN PinOB9: SGMII_HPM_RTL8211_RX_DP PinOB10: GND PinOB11: USB2_SCM_HPM_DN PinOB12: USB2_SCM_HPM_DP PinOB13: GND PinOB14: PECCI_VREF</p> <p>Pin1: CLK_ESPI_CPU0_CLK1 Pin2: ESPI_CPU0_CS_N Pin3: RST_ESPI_CPU0_RSTOUT_N Pin4: ESPI_CPU0_D0 Pin5: ESPI_CPU0_D1 Pin6: ESPI_CPU0_D2 Pin7: ESPI_CPU0_D3 Pin8: ESPI_CPU0_ALERT_N Pin9: SMB_SCM_I2C9_LVC18_SCL Pin10: SMB_SCM_I2C9_LVC18_SDA Pin11: GND Pin12: SCM_TPMRST_LVC18_L Pin13: NC Pin14: HPM_SCM_BIOS_LVC18_COMPLETE Pin15: NC Pin16: SPI_CPU0_SCM_LVC18_D2 Pin17: SPI_CPU0_SCM_LVC18_D3 Pin18: NC Pin19: GND Pin20: NC Pin21: NC Pin22: GND Pin23: NC</p>

Function	Header Reference	Pin Description	
		Pin23: NC Pin24: NC Pin25: GND Pin26: SMB_SCM_I2C7_LVC3_SCL Pin27: SMB_SCM_I2C7_LVC3_SDA Pin28: RST_PLD_DEV_PERST_N Pin29: GND Pin30: P2E_CPU0_P5_RX_BMC_DN Pin31: P2E_CPU0_P5_RX_BMC_DP Pin32: GND Pin33: NC Pin34: NC Pin35: GND Pin36: CLK_100M_SCM_BMC_EP_DN Pin37: CLK_100M_SCM_BMC_EP_DP Pin38: GND Pin39: I3C_BMC_I3C3_LVC1_SCL Pin40: I3C_BMC_I3C3_LVC1_SDA Pin41: I3C_BMC_I3C4_LVC1_SCL Pin42: I3C_BMC_I3C4_LVC1_SDA Pin43: I2C_BMC_CPLD_UPD_SCL Pin44: I2C_BMC_CPLD_UPD_SDA Pin45: NC Pin46: NC Pin47: I2C_BMC_HPM_12_MDC_R_SCL Pin48: I2C_BMC_HPM_12_MDIO_R_SDA A Pin49: SMB_SCM_I2C15_LVC3_SCL Pin50: SMB_SCM_I2C15_LVC3_SDA Pin51: SMB_SCM_I2C8_LVC18_SCL Pin52: SMB_SCM_I2C8_LVC18_SDA Pin53: GND Pin54: SPI_SCM_TPM_LVC18_CLK Pin55: SPI_SCM_TPM_LVC18_CS_N Pin56:	Pin24: NC Pin25: GND Pin26: FM_HPM_SCM_STBY_RDY Pin27: FM_INTRUDER_HDR_BMC_N Pin28: P3V_BAT_CPU0 Pin29: GND Pin30: P2E_CPU0_P5_TX_BMC_DN Pin31: P2E_CPU0_P5_TX_BMC_DP Pin32: GND Pin33: NC Pin34: NC Pin35: GND Pin36: USB2_HPMHOST_BMC_DN Pin37: USB2_HPMHOST_BMC_DP Pin38: GND Pin39: SMB_SCM_HVI3C5_LVC18_SCL Pin40: SMB_SCM_HVI3C5_LVC18_SDA Pin41: NC Pin42: NC Pin43: CLK_50M_SCM_RMII_CLK Pin44: NCSI_HPM_BMC_CRSDV Pin45: NCSI_BMC_HPM_TXEN Pin46: NCSI_BMC_HPM_D0 Pin47: NCSI_BMC_HPM_D1 Pin48: NCSI_HPM_BMC_D0 Pin49: NCSI_HPM_BMC_D1 Pin50: P3V3_AUX_SCM Pin51: UART3_TXD_ASD_PREQ_N Pin52: SGPIO_SCM_HPM_CLK Pin53: SGPIO_SCM_HPM_LD Pin54: SGPIO_SCM_HPM_DOUT Pin55: SGPIO_HPM_SCM_DIN Pin56: UART1_UART5_TXD Pin57: UART1_UART5_RXD Pin58: FM_SCM_PRSENT0_LVC3_N Pin59: BMC_READY Pin60: SPI_CPU0_SCM_LVC18_CLK Pin61: SPI_CPU0_SCM_LVC18_D1 Pin62: SPI_CPU0_SCM_LVC18_D0 Pin63: SPI_CPU0_SCM_LVC18_CS0_N Pin64: GND Pin65: NC Pin66: NC Pin67: GND Pin68: PWRGD_AUX_BMC_CPU0 Pin69: FPGA_BMCRST_L

Function	Header Reference	Pin Description	
		SPI_SCM_TPM_LVC18_MOSI Pin57: SPI_SCM_TPM_LVC18_MISO Pin58: SMB_SCM_I2C1_LVC18_SCL Pin59: SMB_SCM_I2C1_LVC18_SDA Pin60: SPI_BMC_FPGA_LVC18_INT_N Pin61: SMB_SCM_I2C2_LVC18_SCL Pin62: SMB_SCM_I2C2_LVC18_SDA Pin63: UART3_RXD_ASD_PRDY_N Pin64: GND Pin65: NC Pin66: NC Pin67: GND Pin68: NC Pin69: NC Pin70: GND	Pin70: GND
Standard MCIO x4	MCIO0P4A	A Side Pin1: GND Pin2: RX0_P Pin3: RX0_N Pin4: GND Pin5: RX1_P Pin6: RX1_N Pin7: GND Pin8: P3V3_AUX Pin9: NC Pin10: GND Pin11: REFCLKA_P Pin12: REFCLKA_N Pin13: GND Pin14: NC Pin15: NC Pin16: GND Pin17: NC Pin18: NC Pin19: GND Pin20: RX2_P Pin21: RX2_N Pin22: GND Pin23: RX3_P Pin24: RX3_N	B Side Pin1: GND Pin2: TX0_P Pin3: TX0_N Pin4: GND Pin5: TX1_P Pin6: TX1_N Pin7: GND Pin8: MCIO_A_SCL Pin9: MCIO_A_SDA Pin10: GND Pin11: PERST# Pin12: CPRSNT_A_N Pin13: GND Pin14: NC Pin15: NC Pin16: GND Pin17: NC Pin18: NC Pin19: GND Pin20: TX2_P Pin21: TX2_N Pin22: GND Pin23: TX3_P Pin24: TX3_N

Function	Header Reference	Pin Description	
		Pin25: GND Pin26: NC Pin27: NC Pin28: GND Pin29: REFCLKB_P Pin30: REFCLKB_N Pin31: GND Pin32: NC Pin33: NC Pin34: GND Pin35: NC Pin36: NC Pin37: GND	Pin25: GND Pin26: MCIO_B_SCL Pin27: MCIO_B_SDA Pin28: GND Pin29: PERST# Pin30: CPRSNT_B_N Pin31: GND Pin32: NC Pin33: NC Pin34: GND Pin35: NC Pin36: NC Pin37: GND
MCIO from CPU0 MCIO from CPU1	MCIO0P0A, MCIO0P2A, MCIO0P3A MCIO1P0A, MCIO1P2A, MCIO1P3A	A Side Pin1: GND Pin2: RX0_P Pin3: RX0_N Pin4: GND Pin5: RX1_P Pin6: RX1_N Pin7: GND Pin8: P3V3_AUX Pin9: NC Pin10: GND Pin11: REFCLKA_P Pin12: REFCLKA_N Pin13: GND Pin14: RX2_P Pin15: RX2_N Pin16: GND Pin17: RX3_P Pin18: RX3_N Pin19: GND Pin20: RX4_P Pin21: RX4_N Pin22: GND Pin23: RX5_P Pin24: RX5_N Pin25: GND Pin26: NC Pin27: NC Pin28: GND Pin29: USB2_A_P Pin30: USB2_A_N Pin31: GND Pin32: RX6_P Pin33: RX6_N	B Side Pin1: GND Pin2: TX0_P Pin3: TX0_N Pin4: GND Pin5: TX1_P Pin6: TX1_N Pin7: GND Pin8: MCIO_A_SCL Pin9: MCIO_A_SDA Pin10: GND Pin11: PERST# Pin12: CPRSNT_A_N Pin13: GND Pin14: TX2_P Pin15: TX2_N Pin16: GND Pin17: TX3_P Pin18: TX3_N Pin19: GND Pin20: TX4_P Pin21: TX4_N Pin22: GND Pin23: TX5_P Pin24: TX5_N Pin25: GND Pin26: PWRBRK_N Pin27: WAKEB_N Pin28: GND Pin29: NC Pin30: NC Pin31: GND Pin32: TX6_P Pin33: TX6_N

Function	Header Reference	Pin Description	
CPU1		Pin4: GND Pin5: RX1_P Pin6: RX1_N Pin7: GND Pin8: P3V3_AUX Pin9: BP_I2C_ALERT_N Pin10: GND Pin11: REFCLKA0_P Pin12: REFCLKA0_N Pin13: GND Pin14: RX2_P Pin15: RX2_N Pin16: GND Pin17: RX3_P Pin18: RX3_N Pin19: GND Pin20: RX4_P Pin21: RX4_N Pin22: GND Pin23: RX5_P Pin24: RX5_N Pin25: GND Pin26: BP_I2C_SDA Pin27: BP_I2C_SCL Pin28: GND Pin29: REFCLKA1_P / USB2_A_P Pin30: REFCLKA1_N / USB2_A_N Pin31: GND Pin32: RX6_P Pin33: RX6_N Pin34: GND Pin35: RX7_P Pin36: RX7_N Pin37: GND	Pin4: GND Pin5: TX1_P Pin6: TX1_N Pin7: GND Pin8: MCIO_A_SCL Pin9: MCIO_A_SDA Pin10: GND Pin11: PERST# Pin12: CPRSNT_A0_N Pin13: GND Pin14: TX2_P Pin15: TX2_N Pin16: GND Pin17: TX3_P Pin18: TX3_N Pin19: GND Pin20: TX4_P Pin21: TX4_N Pin22: GND Pin23: TX5_P Pin24: TX5_N Pin25: GND Pin26: PWRBRK_N Pin27: WAKEB_N Pin28: GND Pin29: PERST# Pin30: CPRSNT_A1_N Pin31: GND Pin32: TX6_P Pin33: TX6_N Pin34: GND Pin35: TX7_P Pin36: TX7_N Pin37: GND
MCIO from CPU0 MCIO from CPU1	MCIO0P1B, MCIO0G3B MCIO1P1B,	A Side Pin1: GND Pin2: RX8_P Pin3: RX8_N Pin4: GND Pin5: RX9_P Pin6: RX9_N Pin7: GND Pin8: P3V3_AUX Pin9: NC Pin10: GND Pin11: REFCLKB0_P Pin12: REFCLKB0_N	B Side Pin1: GND Pin2: TX8_P Pin3: TX8_N Pin4: GND Pin5: TX9_P Pin6: TX9_N Pin7: GND Pin8: MCIO_B_SCL Pin9: MCIO_B_SDA Pin10: GND Pin11: PERST# Pin12: CPRSNT_BO_N

Function	Header Reference	Pin Description	
		Pin13: GND Pin14: RX10_P Pin15: RX10_N Pin16: GND Pin17: RX11_P Pin18: RX11_N Pin19: GND Pin20: RX12_P Pin21: RX12_N Pin22: GND Pin23: RX13_P Pin24: RX13_N Pin25: GND Pin26: NC Pin27: NC Pin28: GND Pin29: REFCLKB1_P / USB2_B_P Pin30: REFCLKB1_N / USB2_B_N Pin31: GND Pin32: RX14_P Pin33: RX14_N Pin34: GND Pin35: RX15_P Pin36: RX15_N Pin37: GND	Pin13: GND Pin14: TX10_P Pin15: TX10_N Pin16: GND Pin17: TX11_P Pin18: TX11_N Pin19: GND Pin20: TX12_P Pin21: TX12_N Pin22: GND Pin23: TX13_P Pin24: TX13_N Pin25: GND Pin26: PWRBRK_N Pin27: WAKEB_N Pin28: GND Pin29: PERST# Pin30: CPRSNT_B1_N Pin31: GND Pin32: TX14_P Pin33: TX14_N Pin34: GND Pin35: TX15_P Pin36: TX15_N Pin37: GND
MCIO from CPU0	MCIO1G1A	A Side Pin1: GND Pin2: RX0_P Pin3: RX0_N Pin4: GND Pin5: RX1_P Pin6: RX1_N Pin7: GND Pin8: P3V3_AUX Pin9: BP_I2C_ALERT_N Pin10: GND Pin11: REFCLKA0_P Pin12: REFCLKA0_N Pin13: GND Pin14: RX2_P Pin15: RX2_N Pin16: GND Pin17: RX3_P Pin18: RX3_N Pin19: GND Pin20: RX4_P Pin21: RX4_N	B Side Pin1: GND Pin2: TX0_P Pin3: TX0_N Pin4: GND Pin5: TX1_P Pin6: TX1_N Pin7: GND Pin8: MCIO_A_SCL Pin9: MCIO_A_SDA Pin10: GND Pin11: PERST# Pin12: CPRSNT_A0_N Pin13: GND Pin14: TX2_P Pin15: TX2_N Pin16: GND Pin17: TX3_P Pin18: TX3_N Pin19: GND Pin20: TX4_P Pin21: TX4_N

Function	Header Reference	Pin Description	
		Pin22: GND Pin23: RX5_P Pin24: RX5_N Pin25: GND Pin26: BP_I2C_SDA Pin27: BP_I2C_SCL Pin28: GND Pin29: REFCLKA1_P Pin30: REFCLKA1_N Pin31: GND Pin32: RX6_P Pin33: RX6_N Pin34: GND Pin35: RX7_P Pin36: RX7_N Pin37: GND	Pin22: GND Pin23: TX5_P Pin24: TX5_N Pin25: GND Pin26: PWRBRK_N Pin27: WAKEB_N Pin28: GND Pin29: PERST# Pin30: CPRSNT_A1_N Pin31: GND Pin32: TX6_P Pin33: TX6_N Pin34: GND Pin35: TX7_P Pin36: TX7_N Pin37: GND
MCIO from CPU1	MCIO1G1B	A Side Pin1: GND Pin2: RX8_P Pin3: RX8_N Pin4: GND Pin5: RX9_P Pin6: RX9_N Pin7: GND Pin8: P3V3_AUX Pin9: NC Pin10: GND Pin11: REFCLKB0_P Pin12: REFCLKB0_N Pin13: GND Pin14: RX10_P Pin15: RX10_N Pin16: GND Pin17: RX11_P Pin18: RX11_N Pin19: GND Pin20: RX12_P Pin21: RX12_N Pin22: GND Pin23: RX13_P Pin24: RX13_N Pin25: GND Pin26: NC Pin27: NC Pin28: GND Pin29: REFCLKB1_P Pin30: REFCLKB1_N	B Side Pin1: GND Pin2: TX8_P Pin3: TX8_N Pin4: GND Pin5: TX9_P Pin6: TX9_N Pin7: GND Pin8: MCIO_B_SCL Pin9: MCIO_B_SDA Pin10: GND Pin11: PERST# Pin12: CPRSNT_BO_N Pin13: GND Pin14: TX10_P Pin15: TX10_N Pin16: GND Pin17: TX11_P Pin18: TX11_N Pin19: GND Pin20: TX12_P Pin21: TX12_N Pin22: GND Pin23: TX13_P Pin24: TX13_N Pin25: GND Pin26: PWRBRK_N Pin27: WAKEB_N Pin28: GND Pin29: PERST# Pin30: CPRSNT_B1_N

Function	Header Reference	Pin Description	
		Pin31: GND Pin32: RX14_P Pin33: RX14_N Pin34: GND Pin35: RX15_P Pin36: RX15_N Pin37: GND	Pin31: GND Pin32: TX14_P Pin33: TX14_N Pin34: GND Pin35: TX15_P Pin36: TX15_N Pin37: GND